

Project Name: PIBTDL/LC AIO
Project Code: 3PD01Z010001
PCB Number : 14060
PCB Size : 150mmx200mm
PCB Name : LC AIO_Intel BT MB

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15	CPU (POWER) (7/11)		46	(Reserved) GPU:PEC Express (1/5)	
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18	CPU (VSS) (10/11)		49	(Reserved) GPU:GPIO/STRAP (4/5)	
19	CPU (STRAP) (11/11)		50	(Reserved) GPU:PWR/GND (5/5)	
20	(Reserved) DDR3L-SODIMM1		51	(Reserved) GPU DDR3 128MX16	
21	DDR3L-SODIMM2		52	(Reserved) GPU POWER Sequence	
22	(Reserved) Front BD Connector		53	(Reserved) GPU_CTF/PPLAY/LDO/MVDD	
23	AUDIO CODEC-ALC269Q		54	(Reserved) GPU VDDC_NCP81172	
24	Combo Jack & Speaker		55	PWR DCIN JACK	
25	LAN RTL8111GA		56	PWR CPU CORE&VNN	
26	RTS5170 (CARD READER)		57	PWR 5V/3D3V	
27	RUN POWER & SEQUENCE		58	PWR 1D8V_S5	
28	(Reserved) Aspire Link		59	PWR 1D35V_OD675_IPS51363	
29	LCD CONN/CVR		60	PWR CPU 1V_S0&CPU 1V_S5	
30	HDMI OUT		61	PWR 1P5_S0&1P05_S0&1P8V_S0	
31	(Reserved) HDMI IN		62	PWR 12V	

KC.BTD01.29C : Bay Trail-D PENTIUM J2900 4C 2.4G C0
KC.BTD01.19C : Bay Trail-D CELERON J1900 4C 2.0G C0
KC.BTD01.18C : Bay Trail-D CELERON J1800 2C 2.4G C0
KC.29301.BMC : Bay Trail-M CELERON N2930 1.86G

071.00BAY.0C6U : Bay Trail-D PENTIUM J2900 4C 2.4G C0
071.00BAY.0C4U : Bay Trail-D CELERON J1900 4C 2.0G C0
071.00BAY.0C5U : Bay Trail-D CELERON J1800 2C 2.4G C0

XTAL Description				
XTAL	Function	Frequency	Spec	Capacitance
X1801	CPU	25M	+/-30ppm CL:12P	C1814=12pF
				C1815=12pF
X1802	CPU	32.768K	+/-20ppm CL:7P	C1817=4pF
				C1818=4pF
X3	LAN	25M	+/-30ppm CL:12P	C294=15pF
				C295=15pF
X3501	HUB	12M	+/-20ppm CL:20P	C4603=18pF
				C4604=18pF
X5	SCALAR	14.318M	+/-20ppm CL:20P	C532=15pF
				C533=15pF
X7	GPU	27M	+/-30ppm CL:12P	C738=10pF
				C734=10pF

BOM Configuration

O_ : OCP
O6_ : 65W adaptor
O9_ : 90W adaptor
R_ : Reserve
ECIO_ : ITE8732
SIO_ : ITE8772
L18_ : 18 inch Panel
L19_ : 19.5 inch Panel
CMI_ : CHIMEI Panel
ODT_ : ODT Panel

CMI 19.5"
1.L19_
2.SIO_
3.O_
4.O6_
5.CMI_

ODT 18.5"
1.L18_
2.SIO_
3.O_
4.O6_
5.ODT_

CPU: INTEL BAY TRAIL-D
J2900 - KC.BTD01.29C
J1900 - KC.BTD01.19C
J1800 - KC.BTD01.18C

SIO: IT8732F
BX - 71.08732.00E
CX - 71.08732.A0E
SCALAR: RTD2486
71.02486.D0G
LAN: RTL8111GA
71.08111.Y03
Audio Codec: ALC269Q
71.00269.H03
Amplifier: TAS5707
74.05707.01T
USB3.0 redriver: PS8713
71.08713.003
SATA3.0 redriver: PS8520
71.08520.003
LVDS translator: RTD2136
71.02136.B04

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

Cover Page

Size

Document Number

Low Cost AIO

Rev

TA

Date

Friday, September 12, 2014

Sheet

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of

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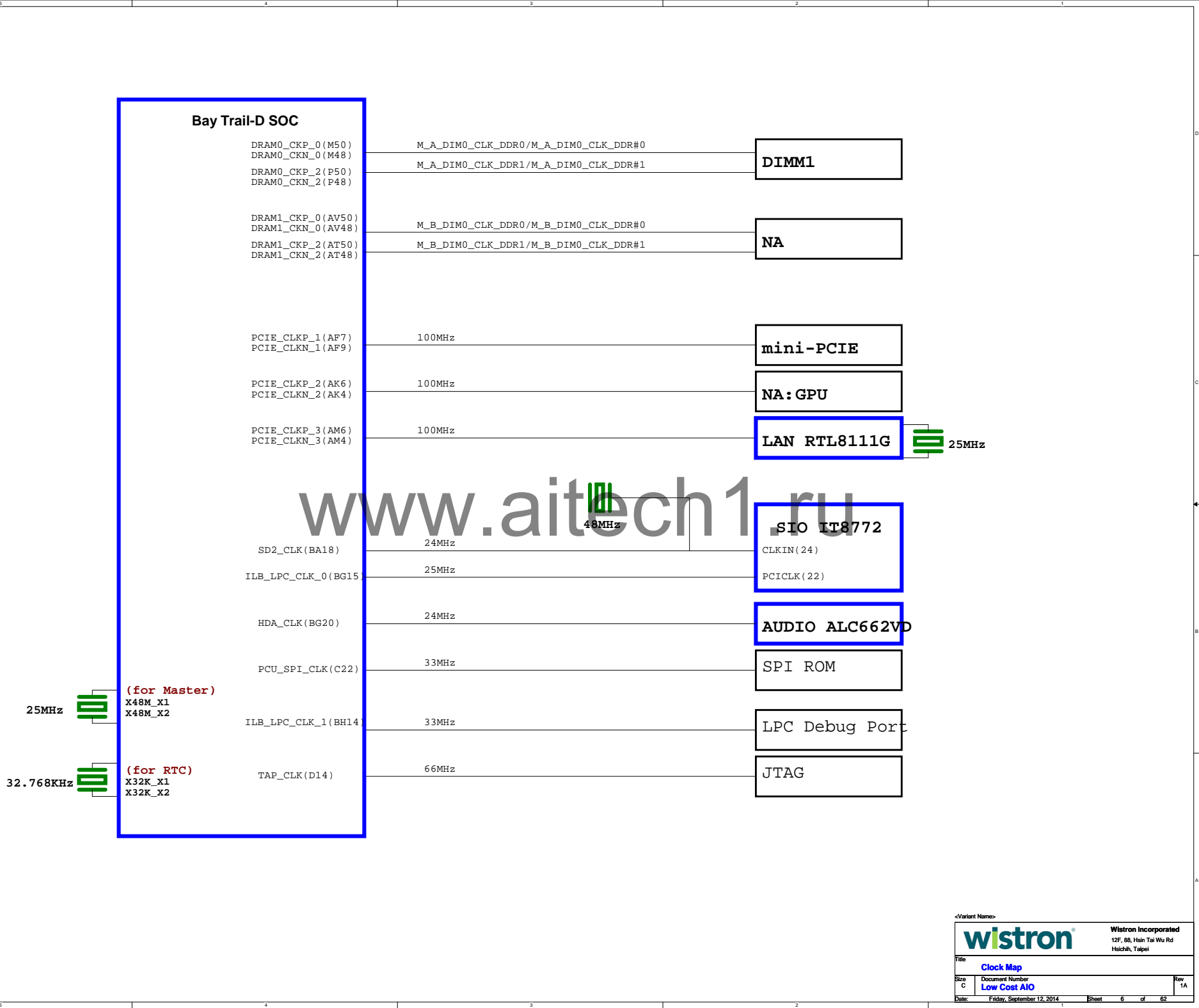
PCB Name : LC AIO Intel BT MB



Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	Reserved

Source	Destination	Signal
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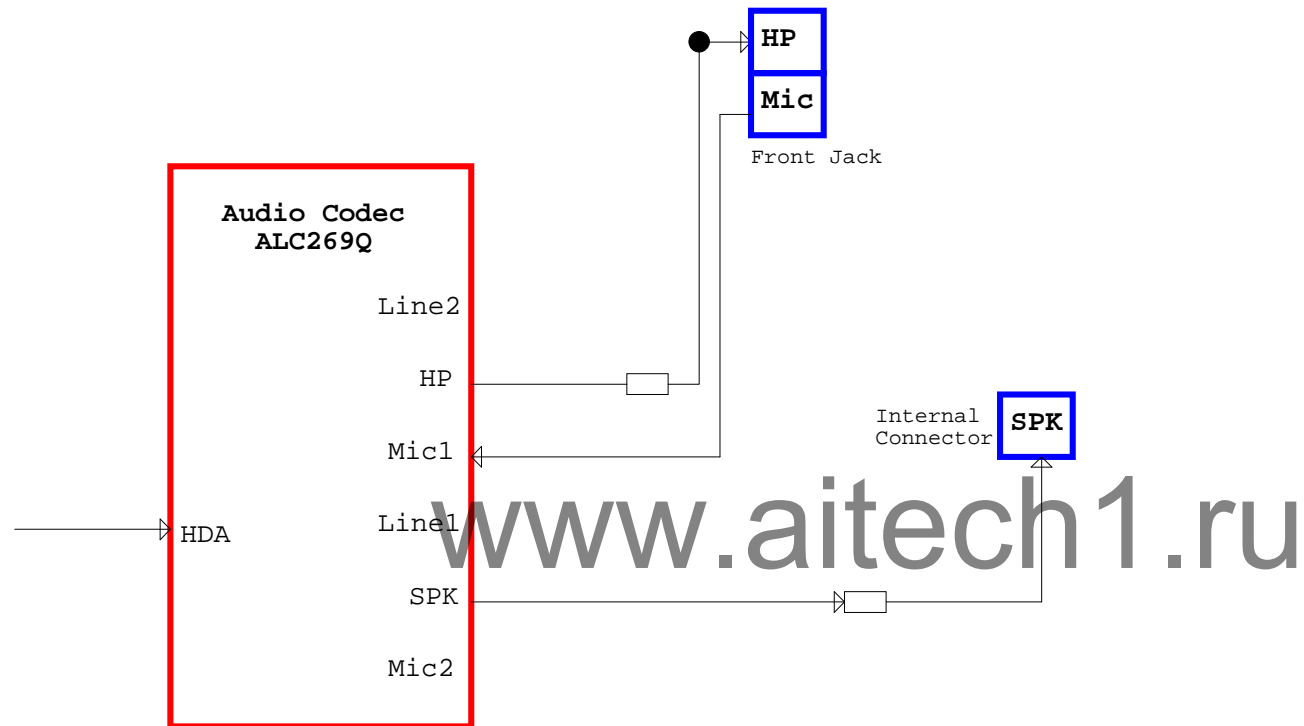


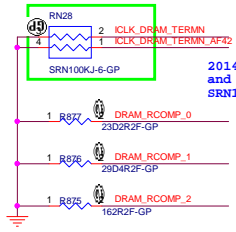
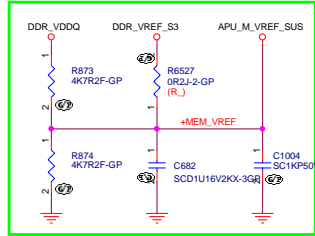
Dallas GPIO Table

Version: 2012/11/27

IC Pin Name	Power Well	Default	Default State	Signal Name	Usage	BIOS Programming					Comment
						S0	S1	S3	S4	S5	
GENINT1_L/GPIO32	VDD_33	null	Input, 15K PU	no use	no use						
GENINT2_L/GPIO33	VDD_33	null	Input, 15K PU	no use	no use						
SCLO/GPIO43	VDD_33	null	Input	SMB0_CLK	SMBUS0	Native	Native	Native	Native	Native	2.2K to 303V_S0
SD_LED/GPIO45	VDD_33	null	Output	no use	no use						
SDAQ/GPIO47	VDD_33	null	Input	SMB0_DATA	SMBUS0	Native	Native	Native	Native	Native	2.2K to 303V_S0
SERIRQ/GPIO48	VDD_33	SERIRQ	Input, 15K PU	SERIRQ_N	SERIRQ	Native	Native	Native	Native	Native	10k(R) to 303V_S0
GPIO49	VDD_33	GPIO49	Input	no use	no use						
GPIO50	VDD_33	GPIO50	Input, 15K PU	KEY0_TEST	BTN test	GPI	GPI	GPI	GPI	GPI	1K to 303V_S0
GPIO51	VDD_33	GPIO51	Input	TP51	no use						
FANOUT0/GPIO52	VDD_33	null	Output, 15K PU	no use	no use						
DEVSPLD0/GPIO55	VDD_33	GPIO55	Input, 15K PU	TP29	no use						
FANIN0/GPIO56	VDD_33	null	Input, 15K PU	no use	no use						
GPIO57	VDD_33	GPIO57	Input, 15K PU	TP48	no use						
GPIO58	VDD_33	GPIO58	Input, 15K PU	TP49	no use						
DEVSPL1/GPIO59	VDD_33	GPIO59	Input, 15K PU	PANEL_OFF_R	panel ON/OFF	GPI	GPI	GPI	GPI	GPI	EC: 10k to 303V_A scalar: 10k to P3P3V
CLK_REQ0_L/SATA_0_S1_L/SATA_ZP0_L/GPIO60	VDD_33	null	Input, 15K PU	BLANCLK_REQ_N_1	clock request (Reserved)						10k(R) to 303V_S0
CLK_REQ1_L/GPIO61	VDD_33	null	Input, 15K PU	CLK_PCIE_WLAN_REQ#	clock request (Reserved)						
CLK_REQ2_L/GPIO62	VDD_33	null	Input, 15K PU	no use	no use						
CLK_REQ3_L/SATA_1_S1_L/SATA_ZP1_L/GPIO63	VDD_33	null	Input, 15K PU	no use	no use						
GPIO64	VDD_33	GPIO64	Input, 15K PU	SMBUS_5P	scalar FW	GPO L	GPO L	GPO L	GPO L	GPO L	100k to GND controlled by SW tool
CLK_REQ0_L/GPIO65/ OSCIN	VDD_33	null	Input, 15K PU	PEG_CLKREQ#	clock request (Reserved)						
SPKR/GPIO66	VDD_33	SPKR	Output	SPKR	beep	Native	Native	Native	Native	Native	
SATA_ACT_L/GPIO67	VDD_33	SATA_ACT_L	Output	no use	no use						
GPIO68	VDD_33	GPIO68	Input, 15K PU	SYS_ID2	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO69	VDD_33	GPIO69	Input, 15K PU	SYS_ID3	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO70	VDD_33	GPIO70	Input, 15K PU	APU_PROCHOT#_R	thermal (Reserved)						1K to 303V_S0
GPIO71	VDD_33	GPIO71	Input	SYS_ID1	SYS ID	GPI	GPI	GPI	GPI	GPI	
SD_CLK/CLK_2/GPIO73	VDD_33	null	Input, 50K PU	no use	no use						
SD_CMD/GPIO74	VDD_33	null	Input, 50K PU	no use	no use						
SD_CD/GPIO75	VDD_33	null	Input, 50K PU	no use	no use						
SD_WP/GPIO76	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA0/SDAT1_2/GPIO77	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA1/SDAT0_2/GPIO78	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA2/GPIO79	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA3/GPIO80	VDD_33	null	Input, 50K PU	no use	no use						
SPI_WP_L/GPIO161	VDD_33_ALW	SPI_WP_L	Input	ROM_RST#	SPI	Native	Native	Native	Native	Native	10k to 303V_S5
SPI_CLK/GPIO162	VDD_33	SPI_CLK	Input, 15K PD	SPI_CLK	SPI	Native	Native	Native	Native	Native	
SPI_DO/GPIO163	VDD_33_ALW	SPI_DO	Input, 15K PD	SPI_DATAOUT	SPI	Native	Native	Native	Native	Native	
SPI_DI/GPIO164	VDD_33_ALW	SPI_DI	Input, 15K PD	SPI_DATAIN	SPI	Native	Native	Native	Native	Native	
SPI_CS1_L/GPIO165	VDD_33	SPI_CS1_L	Input, 15K PU	SPI_CS0_N	SPI	Native	Native	Native	Native	Native	10k to 303V_S5
SPI_CS2_L/GPIO166	VDD_33	SPI_CS2_L	Input, 15K PU	EDID_RDY	EDID for APU	GPI	GPI	GPI	GPI	GPI	10k to 303V_S5
AZ_S0IN0/GPIO167	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN0	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_S0IN1/GPIO168	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN1	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_S0IN2/GPIO169	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN2	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_S0IN3/GPIO170	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN3	AZ	Native	Native	Native	Native	Native	10k(R) to GND
GPIO174	VDD_33_ALW	GPIO 174	Input	Wake#_PCIE	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_S5
IR_LED_L/LB_L/GPIO184	VDD_33_ALW	null	Input, 15K PU	Wake#_LOM	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_S5
SC11/GPIO227	VDD_33_ALW	null	Input	SMB1_CLK	SMBUS1	Native	Native	Native	Native	Native	2.2K to 303V_S5
SDA1/GPIO228	VDD_33_ALW	null	Input	SMB1_DATA	SMBUS1	Native	Native	Native	Native	Native	2.2K to 303V_S5
GA20IN/GEVENT0#	VDD_33	GA20 IN	Input, 15K PU	KA20GATE	GA20IN	Native	Native	Native	Native	Native	10k(R) to 303V_S0
GEVENT2#	VDD_33_ALW	null	Input, 15K PU	SPI_SW	only strapping						strap low
LPC_PME#/ GEVENT3#	VDD_33_ALW	null	Input, 15K PU	PME#_M	LPC	Native	Native	Native	Native	Native	2.2k(R) to 303V_S5
GEVENT4#	VDD_33_ALW	null	Input	THERMAL_SHUT#	thermal (Reserved)						10k(R) to 303V_S5
LPC_PDR/ GEVENT5#	VDD_33_ALW	null	Output	TP_LPC_PDR#	no use						
IR_TX1/ GEVENT6#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT7#	VDD_33_ALW	null	Input	EC_SMI#	(Reserved)						10k to 303V_S5
WAKE#/ GEVENT8#	VDD_33_ALW	null	Input, 15K PU	PCIE_WAKE#	wake up	Native	Native	Native	Native	Native	10k to 303V_S5
SPI_HOLD#/ GEVENT9#	VDD_33_ALW	Strap	Input	SST_HOLD#_1_R	SPI	Native	Native	Native	Native	Native	10k to 303V_S5
GEVENT10#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT11#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC0#/SPI_TPM_CS#/ TRST#/ GEVENT12#	VDD_33_ALW	USB_OC0#	Input, 15K PU	USB_OC_01	USB OCP	Native	Native	Native	Native	Native	10k to 303V_S5
USB_OC1#/TDI/ GEVENT13#	VDD_33_ALW	null	Input, 15K PU	USB_OC_23	USB OCP	Native	Native	Native	Native	Native	10k to 303V_S5
USB_OC2#/TCK/ GEVENT14#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC3#/TDO/ GEVENT15#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
AC_PRES#/IR_RX0/ GEVENT16#	VDD_33_ALW	null	Input, 15K PU	AC_PRES	no use						
GEVENT17#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
BLINK/ GEVENT18#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
SYS_RESET#/ GEVENT19#	VDD_33_ALW	SYS_RESET_L	Input, 15K PU	FP_RST_N	no use						
IR_RX1/ GEVENT20#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
IR_TX0/ GEVENT21#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT22#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
LPC_SMI#/ GEVENT23#	VDD_33_ALW	null	Input, 15K PU	no use	no use						

IC Pin Name	Power Well (GPIO)	Default	Default State	Signal Name	Usage	Open Drain / Push Pull	BIOS Programming					Comment
							S0	S1	S3	S4	S5	
PCIRST3#/GP10	3V5B	PCIRST3#	Native	AMP_PDN#	mute	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_A controlled by EC H: ON, L: OFF/mute
PCIRST2#/GP11	3V5B	PCIRST2#	Native	PCIRST2#	RESET	DO/DI/O	Native	Native	Native	Native	Native	10k(R) to 303V_A
PCIRST1#/GP12	3V5B	PCIRST1#	Native	PCIRST1#	RESET	DO/DI/O	Native	Native	Native	Native	Native	10k(R) to 303V_A
PWROK1/GP13	3V5B	PWROK1	Native	PWROK3_1	PWROK	DO/DI/O	Native	Native	Native	Native	Native	1k to 303V_S0 set delay to 200ms
VCORE_EN/PCH_C1/GP14	3V5B	VCORE_EN	Native	LAN_PWR_EN	LAN power (reserved)	DO/DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	390k to 303V_S5
PCIRST1#N/CIRTX2/GP15/CPU_PG	3V5B	CIRTX2	Native	SIO_PCIRST1#N	RESET	D/DI/O/DI/O/DI/O	Native	Native	Native	Native	Native	10k to 303V_A
SVS8_CTRL#/CIRRX2/GP16	3V5B	SVS8_CTRL#	Native	EC_EUP	EUP	DO/DI/DI/O	Native	Native	Native	Native	Native	10k to 303V_A
RI2H/GP17	3V5B			SPI_WP_N_R_N	SPI WP	DI/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_A H: can write L: write protect
CTS2H/GP20	3V5B	GP20		PANEL_SW_EC	panel ON/OFF	DI/DO	GPI	GPI	GPI	GPI	GPI	10k to 303V_A controlled by EC
DCD2H/GP21	3V5B	GP21		PANEL_CTRL	panel ctrl (reserved)	DI/DO	GPI	GPI	GPI	GPI	GPI	10k to 303V_A controlled by EC
SKC/GP22	3V5B	GP22		SIO_SCK_R	EC EPROM	DO/DI/O	Native	Native	Native	Native	Native	1k to 303V_A
SI/GP23	3V5B	GP23		SIO_SI	EC EPROM	DO/DI/O	Native	Native	Native	Native	Native	1k to 303V_A
RTS2H/GP24	3V5B	GP24		THERMAL_SHUT#_SIO	thermal (reserved)	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k(R) to 303V_S5
DSR2H/GP25	3V5B	GP25		SIO_Audio_Mute	mute (reserved)	DI/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_A
SOUT2/GP26	3V5B	GP26		SIO_UART1_TX	UART	DO/DI/O	Native	Native	Native	Native	Native	10k to 303V_A
SIN2/GP27	3V5B	GP27		SIO_UART1_RX	UART	DI/DO	Native	Native	Native	Native	Native	10k to 303V_A
ATXP/GP30	3V5B	ATXP	Native	SIO_ATXP	sequence	DI/DO	Native	Native	Native	Native	Native	10k to 303V_S0
PWMOUT/GP31	3V5B	PWMOUT	Native	W3_DISABLE_N	wake up	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_S5 L: disable
DPWROK/GP32	3V5B	DPWROK	Native	W1_DISABLE_N	wake up	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_S5 L: disable
SUSACK#/GP33	3V5B	SUSACK#	Native	SIO_BOARD_ID3	board ID	DO/DI/O	GPI	GPI	GPI	GPI	GPI	controlled by EC H: scalar, L: non-scalar
SUSWARN#/GP34	3V5B	SUSWARN#	Native	SIO_BOARD_ID2	board ID	DO/DI/O	GPI	GPI	GPI	GPI	GPI	board stage
FAN_TAC4/GP35	3V5B	FAN_TAC4	Native	SIO_BOARD_ID1	board ID	DI/DO	GPI	GPI	GPI	GPI	GPI	board stage
FAN_CTL3/GP36	3V5B	FAN_CTL3	Native	no use	no use	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	
FAN_TAC3/GP37	3V5B	FAN_TAC3	Native	EC_AMP_RST	mute	DI/DO	GPO L	GPO L	GPO L	GPO H	GPO H	10k to 303V_A controlled by EC H: reset/mute, L: normal
SVSBSW#/GP40	3V5B	SVSBSW#	Native	SLP_S3_N_R3	sequence	DO/DI/O	GPI	GPI	GPI	GPI	GPI	10k to 303V_S5 controlled by EC
PWROK2/GP41	3V5B	PWROK2	Native	PWROK3_2	PWROK (reserved) S0 power (reserved)	DO/DI/O	Native	Native	Native	Native	Native	10k to 303V_S5
PSON#/GP42	3V5B	PSON#	Native	SIO_PSON_N		DO/DI/O	Native	Native	Native	Native	Native	4.7k to 303V_A
PANSW/H#/GP43	3V5B	PANSW/H#	Native	PB_IN_N_1	PWR BTN	DI/DO	Native	Native	Native	Native	Native	330k to 303V_A
PWROK#/GP44	3V5B	PWROK#	Native	SW_ON_N_SIO	sequence	DO/DI/O	Native	Native	Native	Native	Native	10k to 303V_S5
D_RX0/SMCLK2/_GP46	3V5B	null		SMCLK2_SIO	SIO SMBUS2	DI/DO/DI/O	Native	Native	Native	Native	Native	10k to 303V_A controlled by EC
D_TX0/SDMAT2/_GP47	3V5B	null		SMBDAT2_SIO	SIO SMBUS2	DO/DI/DI/O	Native	Native	Native	Native	Native	10k to 303V_A controlled by EC
SO/GP50	3V5B	SO	Native	SIO_SO	EC EPROM	DI/DO	Native	Native	Native	Native	Native	1k to 303V_A
FAN_CTL2/GP51	3V5B	FAN_CTL2	Native	SUSLED_R_N	LED	DO/DI/O	Native	Native	Native	Native	Native	10k to USB30_VCCA
FAN_TAC2/GP52	3V5B	FAN_TAC2	Native	EC_SMI#	(Reserved)	DI/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_S5
SUSCH#/GP53	3V5B	SUSCH#	Native	SLP_S5_N_R	sequence	DI/DO	Native	Native	Native	Native	Native	10k to 303V_S5
PME#/GP54	3V5B	PME#	Native	LPC_PME_N	LPC	DO/DI/O	Native	Native	Native	Native	Native	2.2k(R) to 303V_S5
RSRST#/CIRRX1/GP55	3V5B	RSRST#	Native	ICH_RSMRST_N_R	sequence	DO/DI/DI/O	Native	Native	Native	Native	Native	10k to 303V_S5
MCLK/GP56	3V5B	MCLK	Native	MCLK	no use	DI/DO/DI/O	Native	Native	Native	Native	Native	10k to 5V_S5
MDAT/GP57	3V5B	MDAT	Native	MDAT	no use	DI/DO/DI/O	Native	Native	Native	Native	Native	10k to 5V_S5
KCLK/GP60	3V5B	KCLK	Native	KBCLK	no use	DI/DO/DI/O	Native	Native	Native	Native	Native	10k to 5V_S5
KDAT/GP61	3V5B	KDAT	Native	KDAT	no use	DI/DO/DI/O	Native	Native	Native	Native	Native	10k to 5V_S5
KRST#/GP62	3V5B	KRST#	Native	KBRST_N	KBRST	DO/DI/O	Native	Native	Native	Native	Native	10k(R) to 303V_S0
SLP_SUS#/VLDT_EN/GP63	3V5B	SLP_SUS#	Native	APU_PROCHOT#	(Reserved)	DI/DO/DI/O	GPI	GPI	GPI	GPI	GPI	1k to 303V_S0 controlled by EC
GP70/KSIO	3V5B	KSIO	Native	DET_HDMI	scalar/HDMI	DI/O/DI	GPI	GPI	GPI	GPI	GPI	10k to 303V_A controlled by EC
GP71/KS11	3V5B	KS11	Native	SCALAR_EN	scalar/HDMI	DI/O/DI	GPO H	GPO H	GPO H	GPO L	GPO L	10k to 303V_A controlled by EC H: enable scalar
GP72/KS00	3V5B	KS00	Native	EUP_DSW_SEL	strap	DI/O/DI	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_A
GP73/KS01	3V5B	KS01	Native	SIO_PANEL_ON	panel ON/OFF	DI/O/DI	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_A controlled by EC L: panel ON
GP74/KS02	3V5B	KS02	Native	SIO_PANEL_OFF	panel ON/OFF	DI/O/DI	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 303V_A controlled by EC L: panel OFF
GP75/KS03	3V5B	KS03	Native	LVDS_BLEN_1	panel ON/OFF	DI/O/DI	GPI	GPI	GPI	GPI	GPI	10k to 303V_A controlled by EC
GP76/KS04	3V5B	KS04	Native	no use	no use	DI/O/DI	GPO H	GPO H	GPO H	GPO H	GPO H	
GP77/KS05	3V5B	KS05	Native	SIO_MEM_EVENT_L	power consum. (reserved)	DI/O/DI	GPO H	GPO H	GPO H	GPO H	GPO H	controlled by EC
IO_SCIH/GP85/SDMAT0	3V5B			SIO_SDMAT0	SIO SMBUS0	DO/DI/O/DI/O	Native	Native	Native	Native	Native	4.7k to 303V_S0 controlled by EC
GP86/SMCLK0	3V5B			SIO_SMCLK0	SIO SMBUS0	DI/O/DI/O	Native	Native	Native	Native	Native	4.7k to 303V_S0 controlled by EC

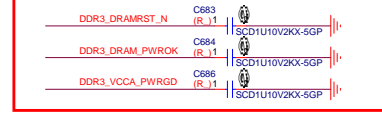




20140509 NICK R871
and R872 merge to
SRN100K

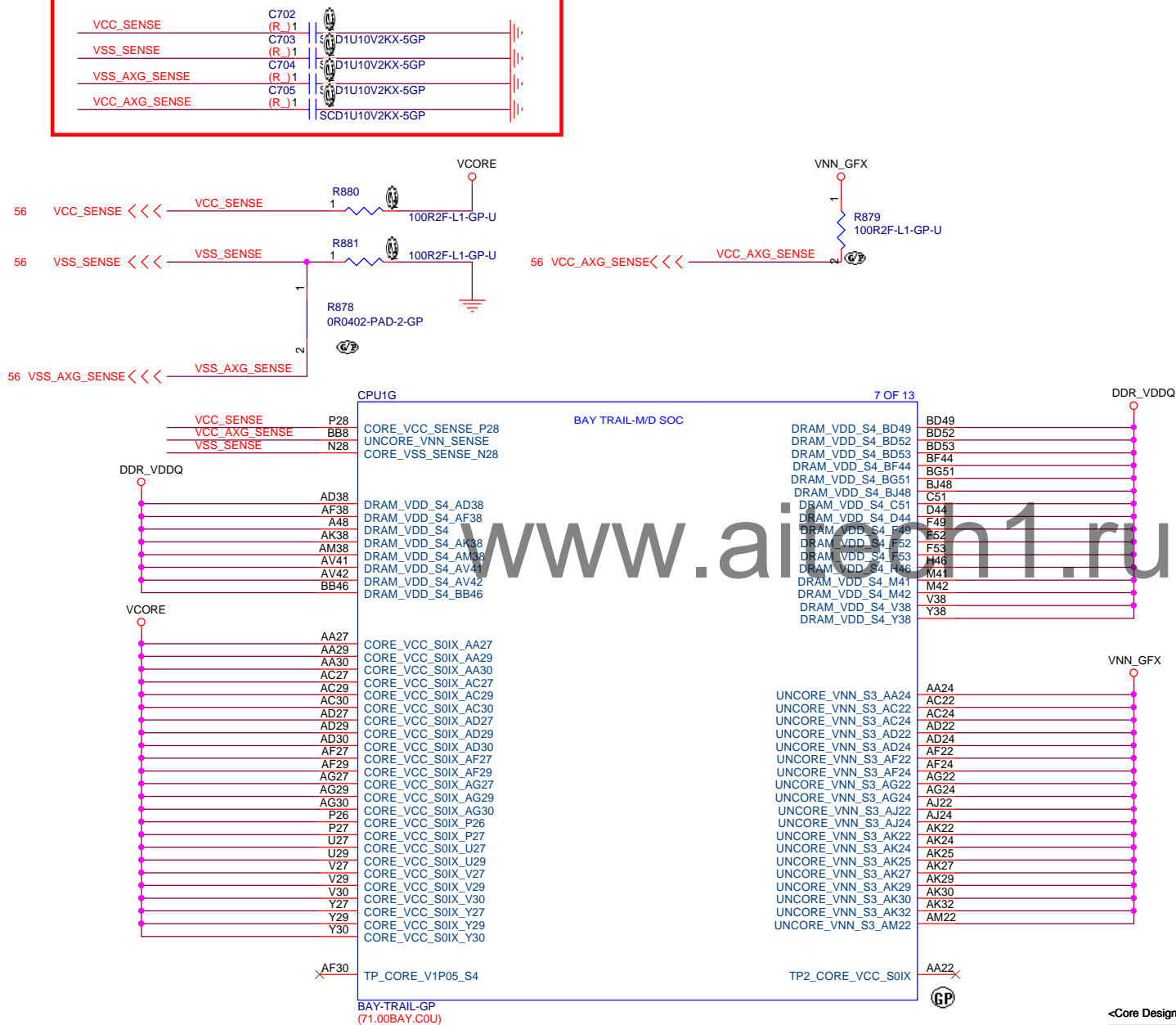
CPU1A				1 OF 13			
BAY TRAIL-M/D SOC				M_DATA_A0			
21 M_MAA_A[15:0]	<<>	M_MAA_A0	K45	DRAM0_MA_0	J36	M_DATA_A1	<<>
		M_MAA_A1	H47	DRAM0_MA_1	P40	M_DATA_A2	
		M_MAA_A2	L41	DRAM0_MA_2	M404	M_DATA_A3	
		M_MAA_A3	H44	DRAM0_MA_3	P36	M_DATA_A4	
		M_MAA_A4	H50	DRAM0_MA_4	N36	M_DATA_A5	
		M_MAA_A5	G53	DRAM0_MA_5	K48	M_DATA_A6	
		M_MAA_A6	H49	DRAM0_MA_6	K42	M_DATA_A7	
		M_MAA_A7	D50	DRAM0_MA_7	B32	M_DATA_A8	
		M_MAA_A8	G52	DRAM0_MA_8	C36	M_DATA_A9	
		M_MAA_A9	E52	DRAM0_MA_9	C36	M_DATA_A10	
		M_MAA_A10	K48	DRAM0_MA_10	C37	M_DATA_A11	
		M_MAA_A11	E51	DRAM0_MA_11	C37	M_DATA_A12	
		M_MAA_A12	F47	DRAM0_MA_12	C37	M_DATA_A13	
		M_MAA_A13	J51	DRAM0_MA_13	C37	M_DATA_A14	
		M_MAA_A14	B49	DRAM0_MA_14	C37	M_DATA_A15	
		M_MAA_A15	B50	DRAM0_MA_15	C37	M_DATA_A16	
21 M_MA_DM[7:0]	<<>	M_MA_DM0	G36	DRAM0_DM_0	F42	M_DATA_A17	
		M_MA_DM1	B36	DRAM0_DM_1	F42	M_DATA_A18	
		M_MA_DM2	F38	DRAM0_DM_2	F42	M_DATA_A19	
		M_MA_DM3	B42	DRAM0_DM_3	F42	M_DATA_A20	
		M_MA_DM4	P51	DRAM0_DM_4	F42	M_DATA_A21	
		M_MA_DM5	V42	DRAM0_DM_5	F42	M_DATA_A22	
		M_MA_DM6	Y50	DRAM0_DM_6	F42	M_DATA_A23	
		M_MA_DM7	Y52	DRAM0_DM_7	F42	M_DATA_A24	
21 M_RAS_A_N	>>>	M_RAS_A_N	M45	DRAM0_RAS	F42	M_DATA_A25	
21 M_CAS_A_N	>>>	M_CAS_A_N	M45	DRAM0_CAS	F42	M_DATA_A26	
21 M_WE_A_N	>>>	M_WE_A_N	H51	DRAM0_WE	F42	M_DATA_A27	
21 M_SBS_A0	>>>	M_SBS_A0	K47	DRAM0_BS_0	F42	M_DATA_A28	
21 M_SBS_A1	>>>	M_SBS_A1	K44	DRAM0_BS_1	F42	M_DATA_A29	
21 M_SBS_A2	>>>	M_SBS_A2	D52	DRAM0_BS_2	F42	M_DATA_A30	
21 M_SCS_A_N0	<<<	M_SCS_A_N0	P44	DRAM0_CS_0	F42	M_DATA_A31	
21 M_SCS_A_N1	<<<	M_SCS_A_N1	P45	DRAM0_CS_1	F42	M_DATA_A32	
21 M_SCKE_A0	<<<	M_SCKE_A0	C47	DRAM0_CKE_0	F42	M_DATA_A33	
21 M_SCKE_A1	<<<	M_SCKE_A1	F44	RESERVED_D48	F42	M_DATA_A34	
21 M_ODT_A0	<<<	M_ODT_A0	T41	DRAM0_ODT_0	F42	M_DATA_A35	
21 M_ODT_A1	<<<	M_ODT_A1	P42	DRAM0_ODT_1	F42	M_DATA_A36	
21 CK_M_DDR0_A_DP	<<<	CK_M_DDR0_A_DP	M50	DRAM0_CKP_0	F42	M_DATA_A37	
21 CK_M_DDR0_A_DN	<<<	CK_M_DDR0_A_DN	M48	DRAM0_CKN_0	F42	M_DATA_A38	
21 CK_M_DDR1_A_DP	<<<	CK_M_DDR1_A_DP	P50	DRAM0_CKP_2	F42	M_DATA_A39	
21 CK_M_DDR1_A_DN	<<<	CK_M_DDR1_A_DN	P48	DRAM0_CKN_2	F42	M_DATA_A40	
21 DDR3_DRAMRST_N	<<<	DDR3_DRAMRST_N	P41	DRAM0_DRAMRST	F42	M_DATA_A41	
APU_M_VREF_SUS	<<<	DRAM_VREF	AF44	DRAM_VREF	F42	M_DATA_A42	
13 DDR3_DRAM_PWRKOK	>>>	DDR3_DRAM_PWRKOK	AD42	DRAM_VDD_S4_PWRKOK	F42	M_DATA_A43	
13 DDR3_VCCA_PWRGD	>>>	DDR3_VCCA_PWRGD	AB42	DRAM_CORE_PWRKOK	F42	M_DATA_A44	
DRAM_RCOMP_0	<<<	DRAM_RCOMP_0	AD44	RESERVED_AF40	F42	M_DATA_A45	
DRAM_RCOMP_1	<<<	DRAM_RCOMP_1	AF45	RESERVED_AF41	F42	M_DATA_A46	
DRAM_RCOMP_2	<<<	DRAM_RCOMP_2	AD45	RESERVED_AD40	F42	M_DATA_A47	
			AF40	RESERVED_AD41	F42	M_DATA_A48	
			AD40		F42	M_DATA_A49	
			AD41		F42	M_DATA_A50	
					F42	M_DATA_A51	
					F42	M_DATA_A52	
					F42	M_DATA_A53	
					F42	M_DATA_A54	
					F42	M_DATA_A55	
					F42	M_DATA_A56	
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					F42	M_DATA_A59	
					F42	M_DATA_A60	
					F42	M_DATA_A61	
					F42	M_DATA_A62	
					F42	M_DATA_A63	
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					F42	M_DATA_A93	
					F42	M_DATA_A94	
					F42	M_DATA_A95	
					F42	M_DATA_A96	
					F42	M_DATA_A97	
					F42	M_DATA_A98	
					F42	M_DATA_A99	
					F42	M_DATA_A100	

reserve the 0402 0.1u caps on reset for EMI.



CPU1B				2 OF 13			
BAY TRAIL-M/D SOC				M_DATA_A0			
21 M_MAA_A[15:0]	<<>	M_MAA_A0	K45	DRAM1_MA_0	J36	M_DATA_A1	<<>
		M_MAA_A1	H47	DRAM1_MA_1	P40	M_DATA_A2	
		M_MAA_A2	L41	DRAM1_MA_2	M404	M_DATA_A3	
		M_MAA_A3	H44	DRAM1_MA_3	P36	M_DATA_A4	
		M_MAA_A4	H50	DRAM1_MA_4	N36	M_DATA_A5	
		M_MAA_A5	G53	DRAM1_MA_5	K48	M_DATA_A6	
		M_MAA_A6	H49	DRAM1_MA_6	K42	M_DATA_A7	
		M_MAA_A7	D50	DRAM1_MA_7	B32	M_DATA_A8	
		M_MAA_A8	G52	DRAM1_MA_8	C36	M_DATA_A9	
		M_MAA_A9	E52	DRAM1_MA_9	C36	M_DATA_A10	
		M_MAA_A10	K48	DRAM1_MA_10	C37	M_DATA_A11	
		M_MAA_A11	E51	DRAM1_MA_11	C37	M_DATA_A12	
		M_MAA_A12	F47	DRAM1_MA_12	C37	M_DATA_A13	
		M_MAA_A13	J51	DRAM1_MA_13	C37	M_DATA_A14	
		M_MAA_A14	B49	DRAM1_MA_14	C37	M_DATA_A15	
		M_MAA_A15	B50	DRAM1_MA_15	C37	M_DATA_A16	
21 M_MA_DM[7:0]	<<>	M_MA_DM0	G36	DRAM1_DM_0	F42	M_DATA_A17	
		M_MA_DM1	B36	DRAM1_DM_1	F42	M_DATA_A18	
		M_MA_DM2	F38	DRAM1_DM_2	F42	M_DATA_A19	
		M_MA_DM3	B42	DRAM1_DM_3	F42	M_DATA_A20	
		M_MA_DM4	P51	DRAM1_DM_4	F42	M_DATA_A21	
		M_MA_DM5	V42	DRAM1_DM_5	F42	M_DATA_A22	
		M_MA_DM6	Y50	DRAM1_DM_6	F42	M_DATA_A23	
		M_MA_DM7	Y52	DRAM1_DM_7	F42	M_DATA_A24	
21 M_RAS_A_N	>>>	M_RAS_A_N	M45	DRAM1_RAS	F42	M_DATA_A25	
21 M_CAS_A_N	>>>	M_CAS_A_N	M45	DRAM1_CAS	F42	M_DATA_A26	
21 M_WE_A_N	>>>	M_WE_A_N	H51	DRAM1_WE	F42	M_DATA_A27	
21 M_SBS_A0	>>>	M_SBS_A0	K47	DRAM1_BS_0	F42	M_DATA_A28	
21 M_SBS_A1	>>>	M_SBS_A1	K44	DRAM1_BS_1	F42	M_DATA_A29	
21 M_SBS_A2	>>>	M_SBS_A2	D52	DRAM1_BS_2	F42	M_DATA_A30	
21 M_SCS_A_N0	<<<	M_SCS_A_N0	P44	DRAM1_CS_0	F42	M_DATA_A31	
21 M_SCS_A_N1	<<<	M_SCS_A_N1	P45	DRAM1_CS_1	F42	M_DATA_A32	
21 M_SCKE_A0	<<<	M_SCKE_A0	C47	DRAM1_CKE_0	F42	M_DATA_A33	
21 M_SCKE_A1	<<<	M_SCKE_A1	F44	RESERVED_BE46	F42	M_DATA_A34	
21 M_ODT_A0	<<<	M_ODT_A0	T41	DRAM1_ODT_0	F42	M_DATA_A35	
21 M_ODT_A1	<<<	M_ODT_A1	P42	DRAM1_ODT_1	F42	M_DATA_A36	
21 CK_M_DDR0_A_DP	<<<	CK_M_DDR0_A_DP	M50	DRAM1_CKP_0	F42	M_DATA_A37	
21 CK_M_DDR0_A_DN	<<<	CK_M_DDR0_A_DN	M48	DRAM1_CKN_0	F42	M_DATA_A38	
21 CK_M_DDR1_A_DP	<<<	CK_M_DDR1_A_DP	P50	DRAM1_CKP_2	F42	M_DATA_A39	
21 CK_M_DDR1_A_DN	<<<	CK_M_DDR1_A_DN	P48	DRAM1_CKN_2	F42	M_DATA_A40	
21 DDR3_DRAMRST_N	<<<	DDR3_DRAMRST_N	P41	DRAM1_DRAMRST	F42	M_DATA_A41	
APU_M_VREF_SUS	<<<	DRAM_VREF	AF44	DRAM_VREF	F42	M_DATA_A42	
13 DDR3_DRAM_PWRKOK	>>>	DDR3_DRAM_PWRKOK	AD42	DRAM_VDD_S4_PWRKOK	F42	M_DATA_A43	
13 DDR3_VCCA_PWRGD	>>>	DDR3_VCCA_PWRGD	AB42	DRAM_CORE_PWRKOK	F42	M_DATA_A44	
DRAM_RCOMP_0	<<<	DRAM_RCOMP_0	AD44	RESERVED_AF40	F42	M_DATA_A45	
DRAM_RCOMP_1	<<<	DRAM_RCOMP_1	AF45	RESERVED_AF41	F42	M_DATA_A46	
DRAM_RCOMP_2	<<<	DRAM_RCOMP_2	AD45	RESERVED_AD40	F42	M_DATA_A47	
			AF40	RESERVED_AD41	F42	M_DATA_A48	
			AD40		F42	M_DATA_A49	
			AD41		F42	M_DATA_A50	
					F42	M_DATA_A51	
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					F42	M_DATA_A96	
					F42	M_DATA_A97	
					F42	M_DATA_A98	
					F42	M_DATA_A99	
					F42	M_DATA_A100	

reserve the 0402 0.1u caps on reset for EMI



<Core Design>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

CPU (VCC CORE)

Size

Document Number

Custom

Low Cost AIO

Rev

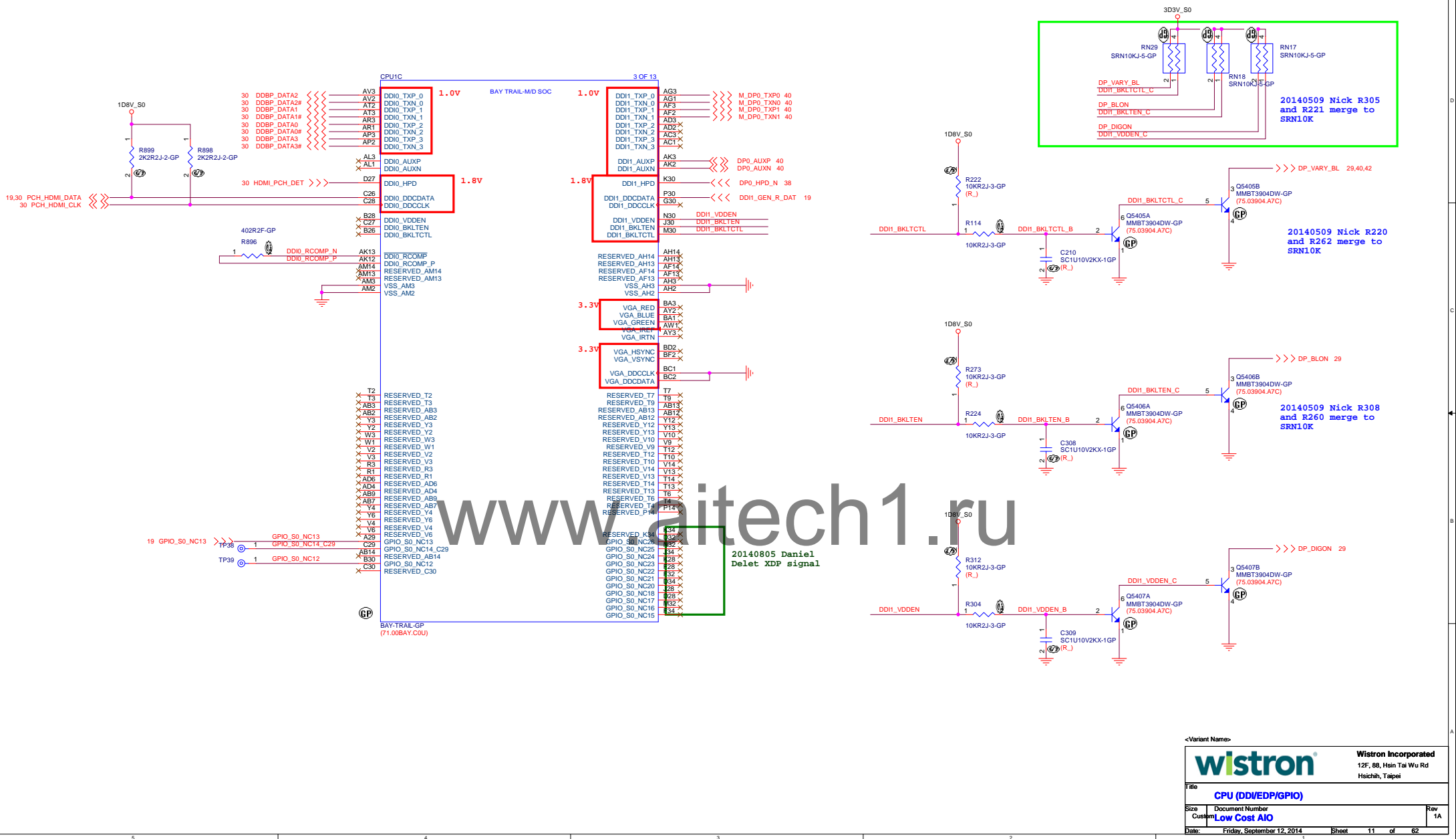
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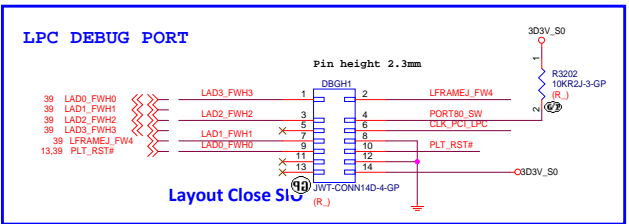
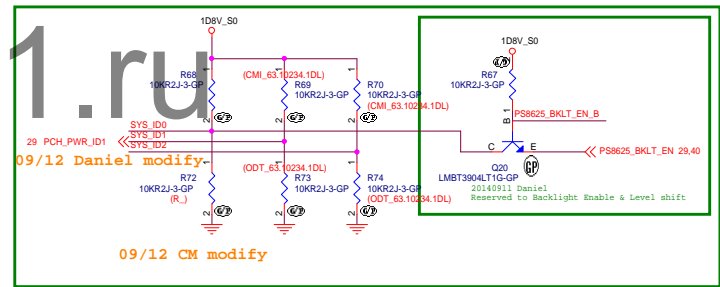
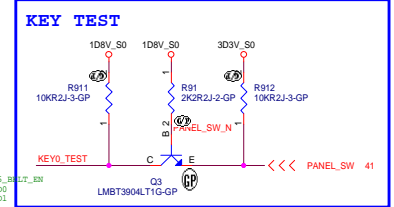
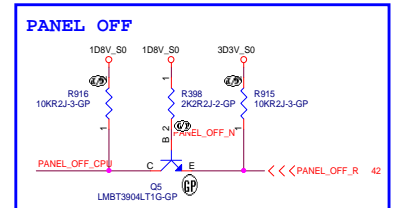
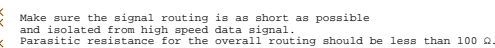
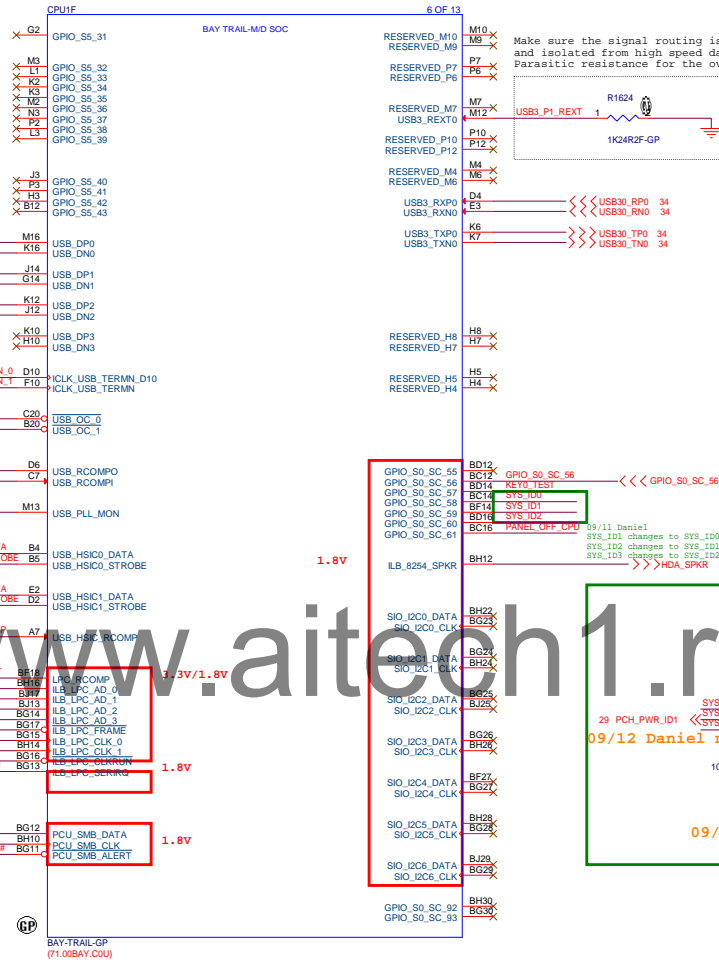
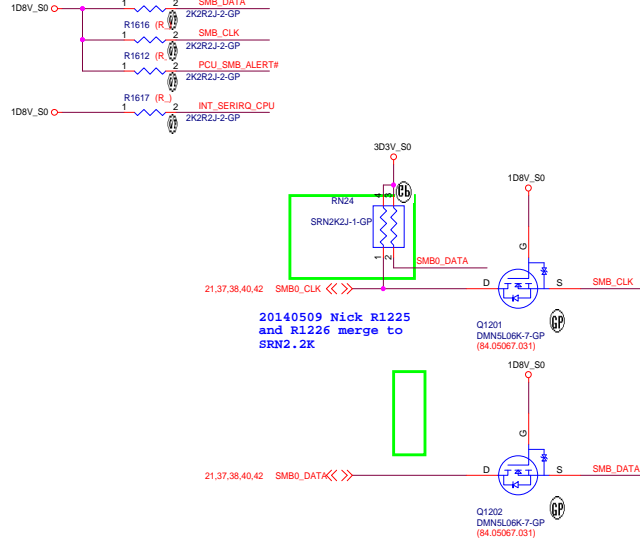
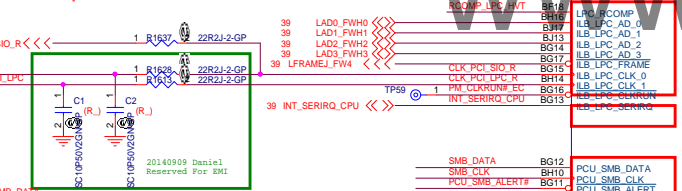
Friday, September 12, 2014

Sheet

10 of 62



Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	Delete TOUCH1



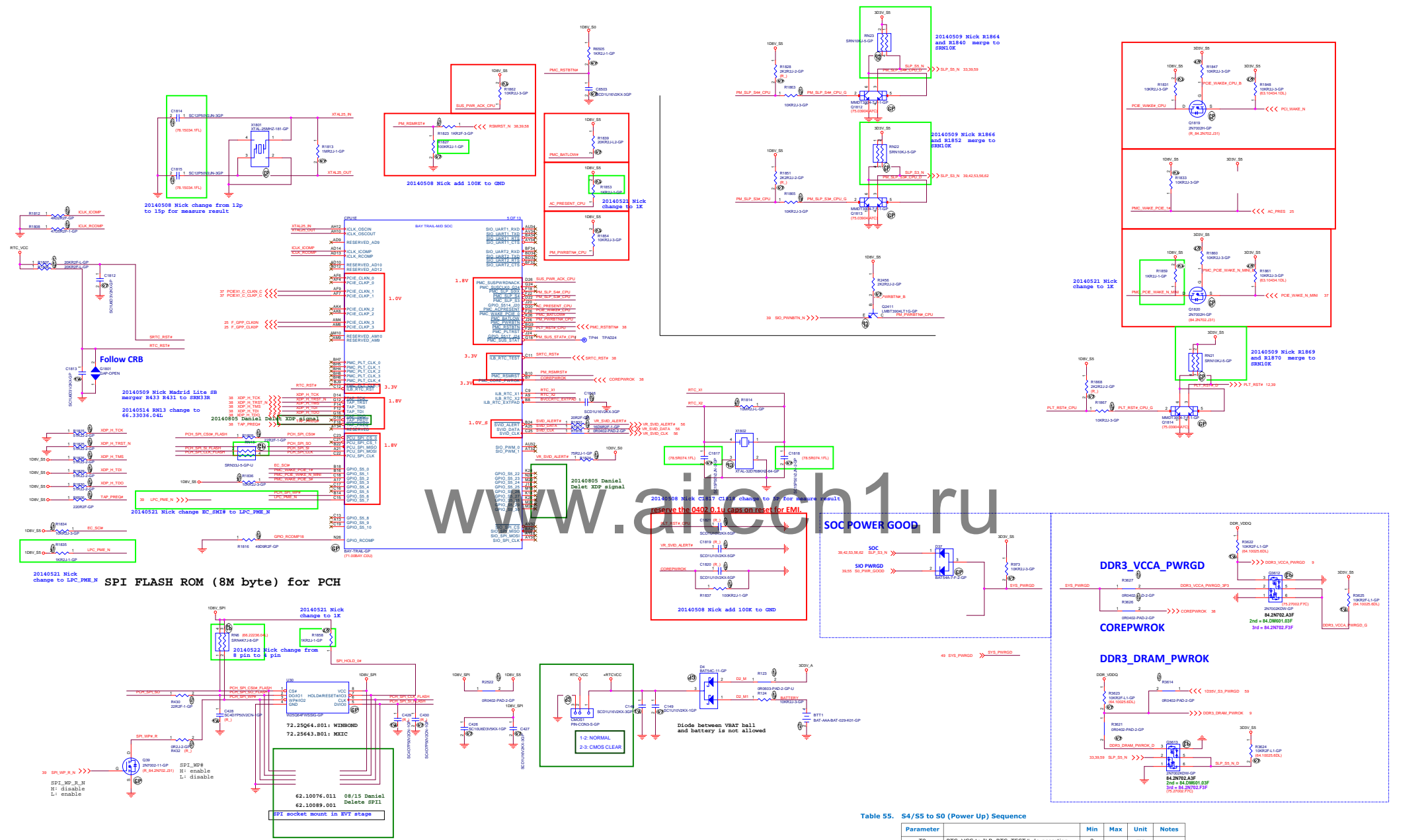
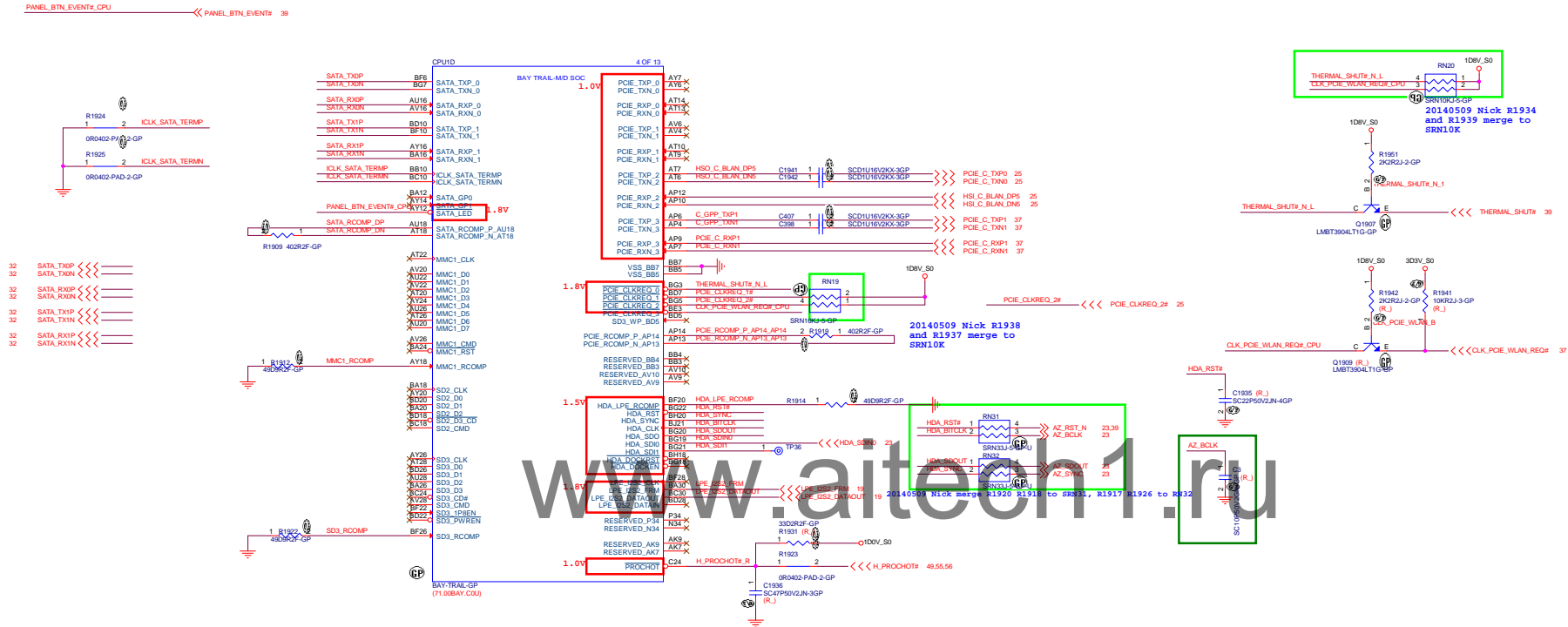


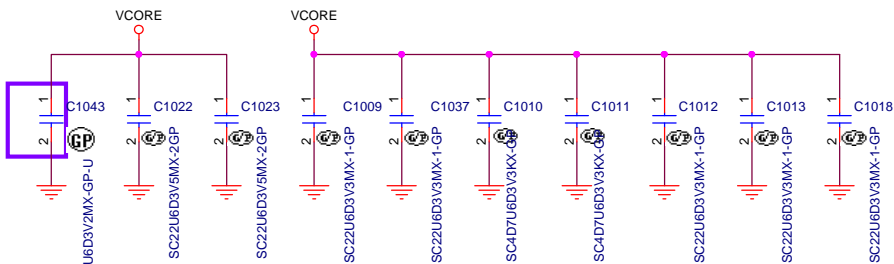
Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter	Min	Max	Unit	Notes
T0				RTC_VCC to ILB_RTC_TEST# de-assertion
T1		9	ms	V3P3A valid to PMIC_RST# de-assertion
T2		100	ms	Core well stable to DRAM_CORE_PWRON and PMIC_CORE_PWRON assertion
T3				

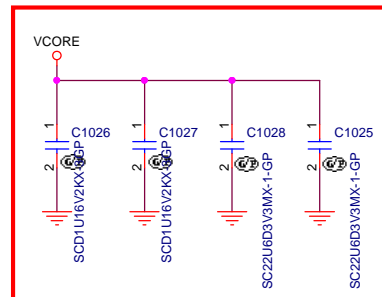
20140807 Daniel
Short PANEL_BTN_EVENT# to PANEL_BTN_EVENT#_CPU
Delete Q1816, R1856, R1855"



VCORE

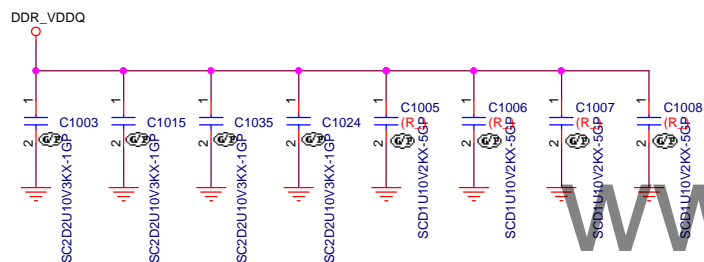


reserve the 0402 0.1u caps
on reset for EMI(5/9).

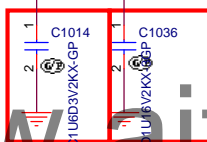


20150515 Nick add for power request

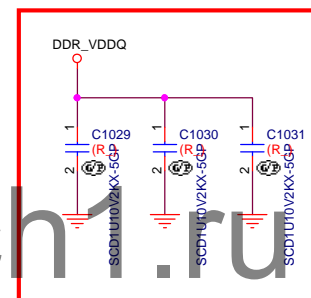
DDR_VDDQ



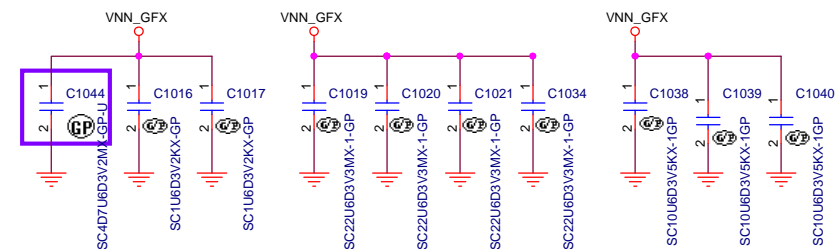
close to pin AD38 & AF38



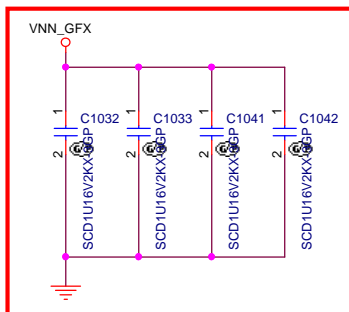
reserve the 0402 0.1u caps
on reset for EMI(5/9).



VNN_GFX



reserve the 0402 0.1u caps
on reset for EMI(5/9).



20150515 Nick add for power request

<Core Design>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

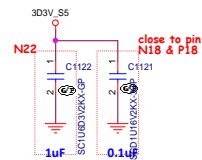
Title
CPU (POWER CAP1)

Size B Document Number
Low Cost A10

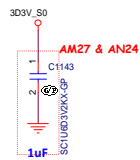
Rev
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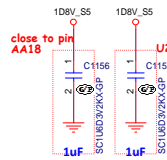
3D3V_S5



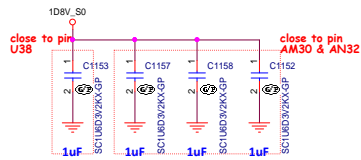
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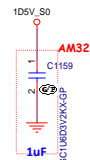
1D8V_S5



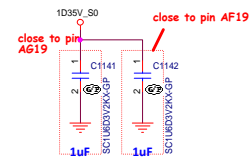
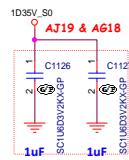
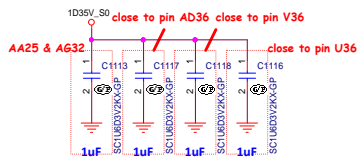
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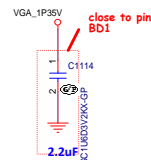
1D5V_S0



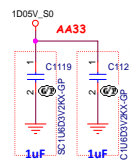
1D35V_S0



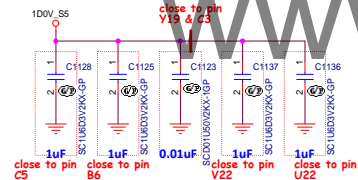
VGA_1P35V



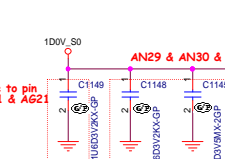
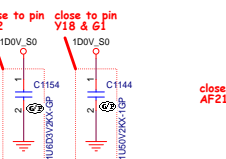
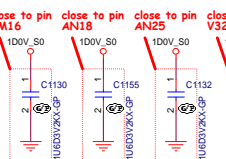
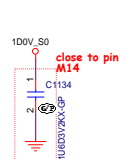
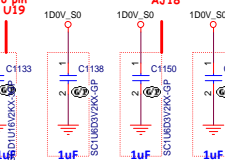
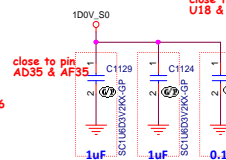
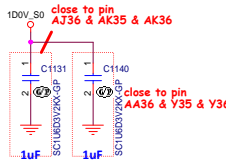
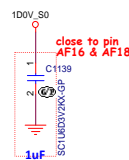
1D05V_S0



1D0V_S5



1D0V_S0



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Hsinchu, Taipei

File
CPU (POWER CAP2)

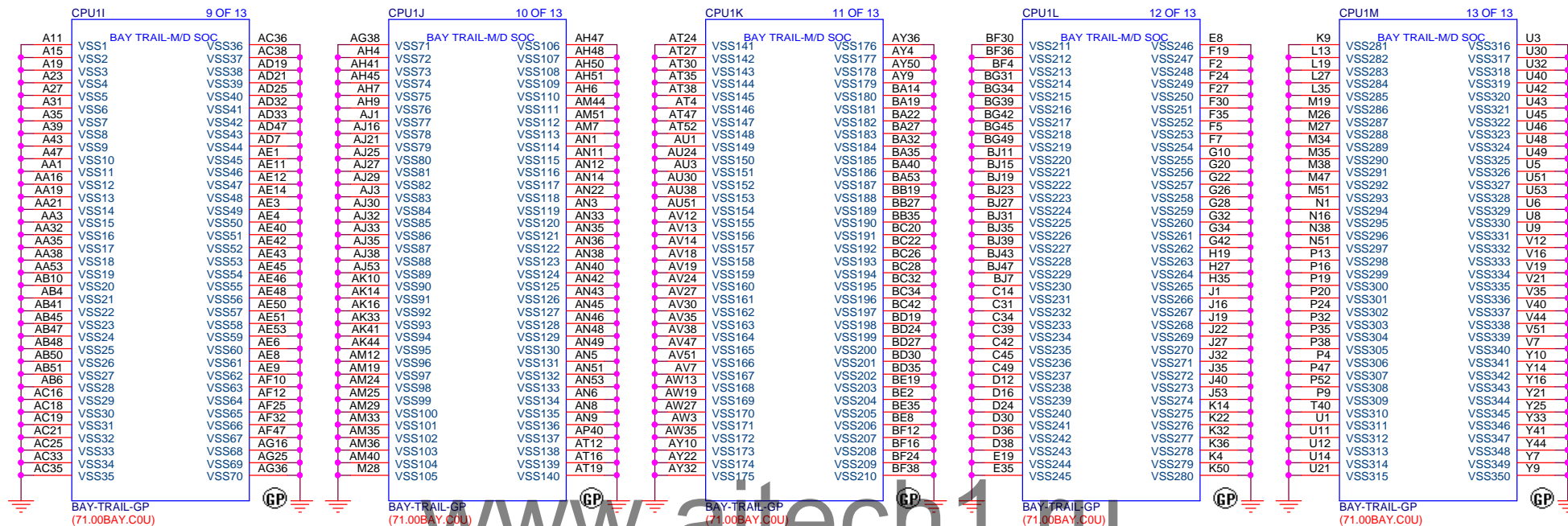
Size
Custom

Document Number
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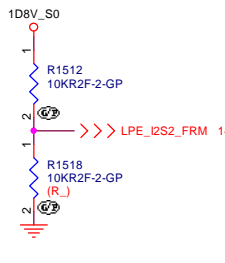
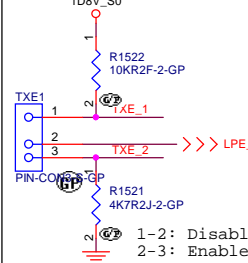
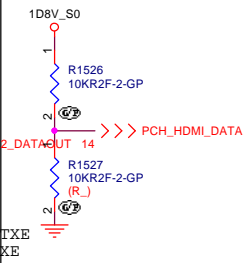
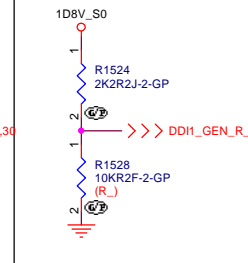
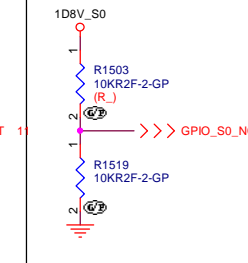
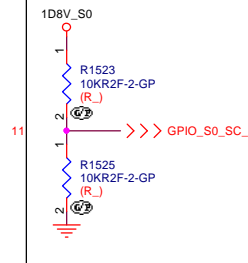
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CPU (VSS)		
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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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CPU (STRAP)

Size
A3

Document Number
Low Cost AIO

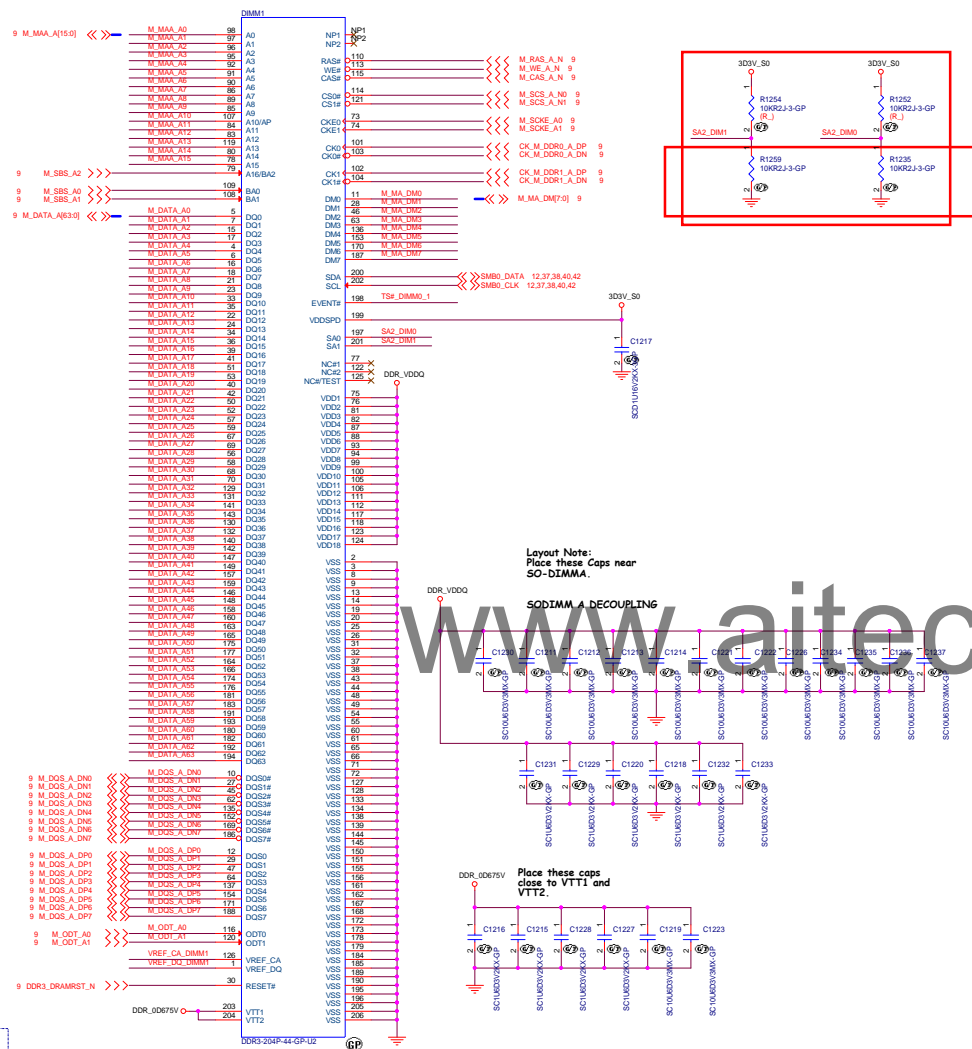
Rev
1A

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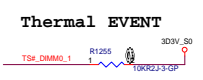
TBD

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Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

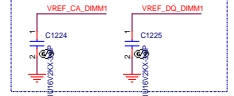


Layout Note:
Place these Caps near SO-DIMMA.

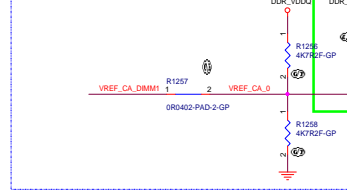
SODIMM A DECOUPLING

Place these caps close to VTT1 and VTT2.

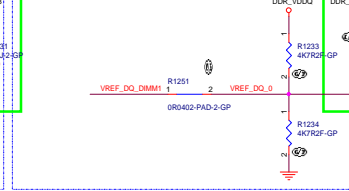
Close DIMM1 CA & DQ pin



For Intel Recommend Close to DIMM1 (Bay Trail)



For Intel Recommend Close to DIMM1 (Bay Trail)



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Title

Front BD Connector

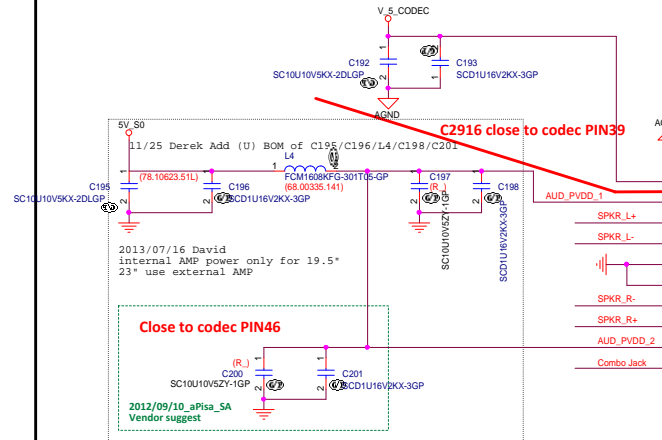
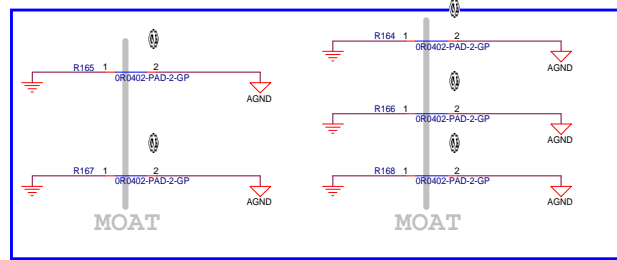
Size
A

Document Number
Low Cost AIO

Rev
1A

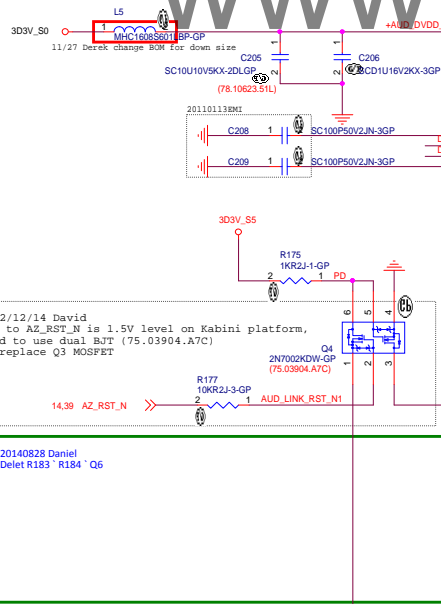
Date: Friday, September 12, 2014

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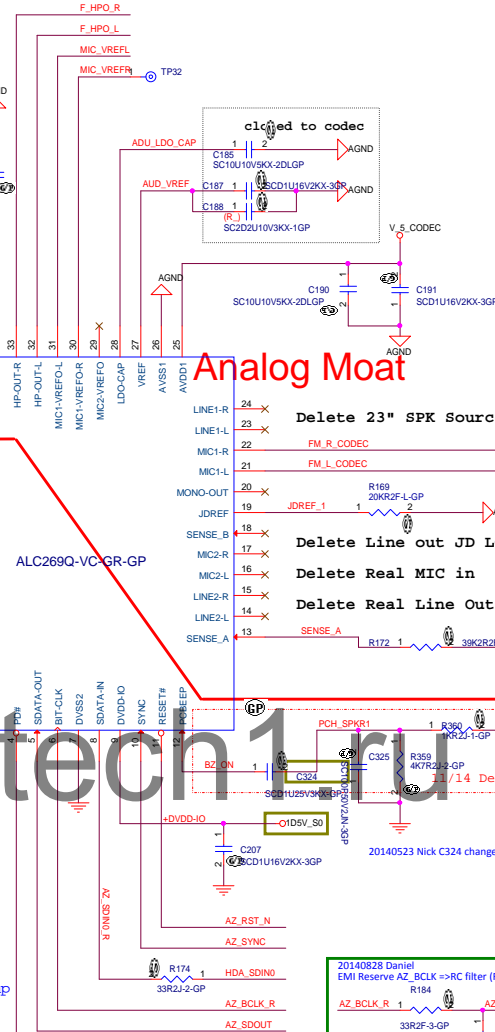
- 14 HDA_SDI0
- 14 AZ_SDIOUT
- 14.39 AZ_RST_N
- 14 AZ_SYNC
- 14 AZ_BCLK
- 36 DMIC_DATA
- 36 DMIC_CLK
- 12 HDA_SPKR
- 24 SPKR_L+
- 24 SPKR_L-
- 24 SPKR_R+
- 24 SPKR_R-
- 24 MIC_VREFL
- 24 F_HPO_R
- 24 F_HPO_L
- 24 FM_L_CODEC
- 24 FM_R_CODEC
- 24 JD_HP_R
- 24 Combo Jack

Digital Moat



20140828 Daniel
Delet R183 `R184` Q6

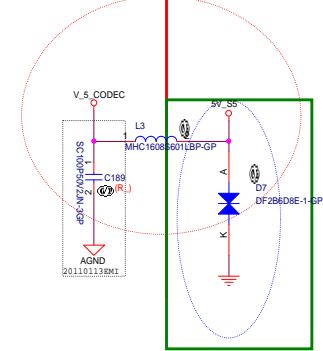
Internal AMP
H: no mute
L: mute



Analog Moat

- Delete 23" SPK Source
- FM_R_CODEC
- FM_L_CODEC
- MONO-OUT
- JDREF
- SENSE_B
- MIC2-R
- MIC2-L
- LINE2-R
- LINE2-L
- SENSE_A

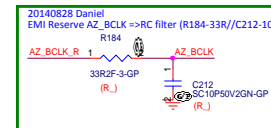
Analog Moat Digital Moat



20140818 Daniel
D7 Change symbol 75.0DF2B.077

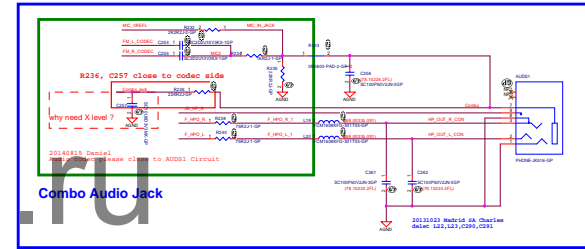
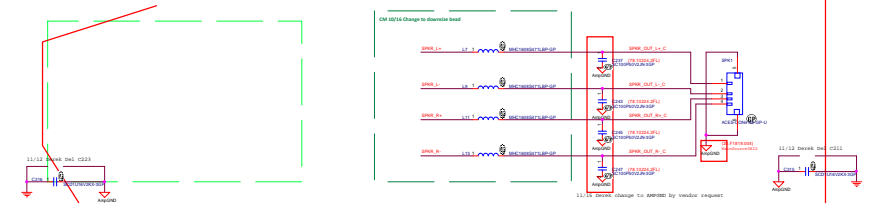
20121007 aPisa Charles
Only MIC1 can use for combo function

Bogis 20140128
Change R360 to 1Kohm
Change C324 to 0.1uF
schematic and link SPKR to codec IC



Support iPhone ~ Mount R3018,R3020
unMount R3019,R3021

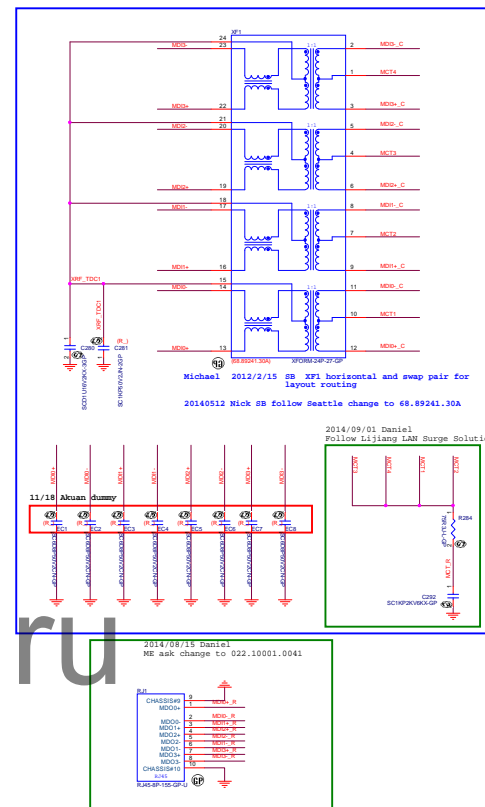
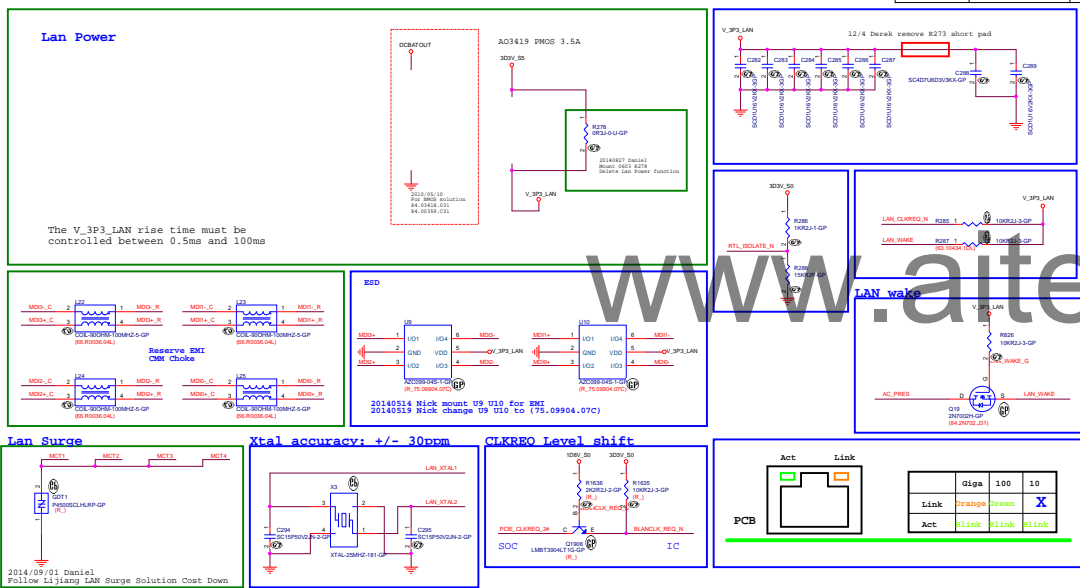
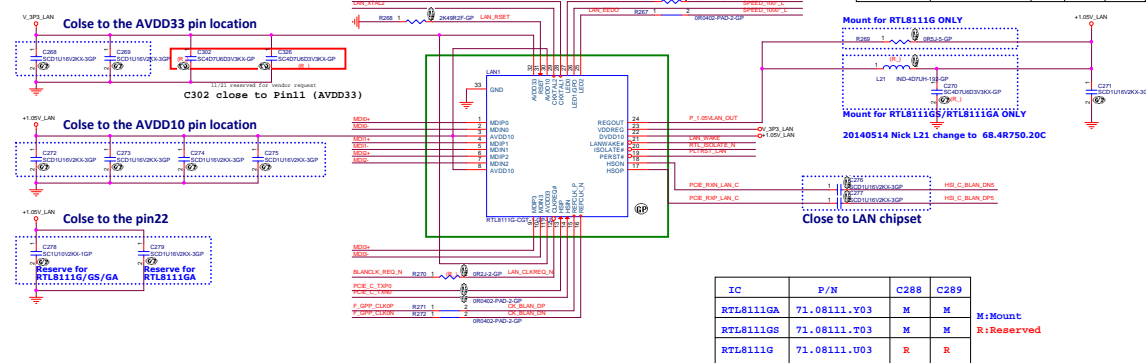
Support Nokia ~ Mount R3019,R3021
unMount R3018,R3020

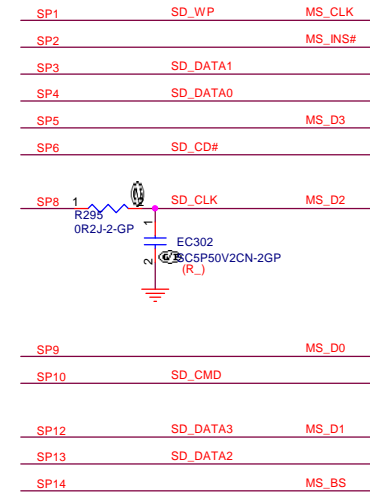
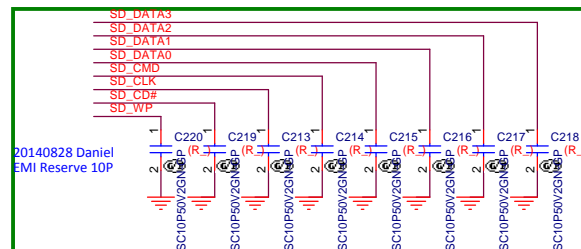
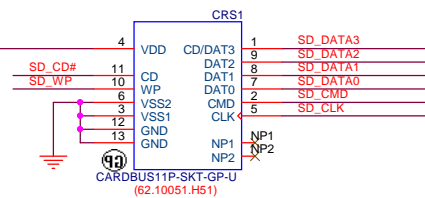
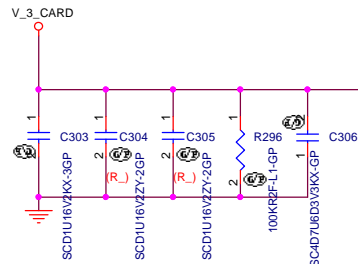


NOTE: NOTE_AP_CTL
When the PC mode and Monitor
mode are being switched
NOTE_AP_CTL should be low
in order to avoid the noise
NOTE_AP_CTL also control when
switch NOTE in the PC mode or
Monitor mode
NOTE_AP_CTL also control when
system wake from S3 to S0

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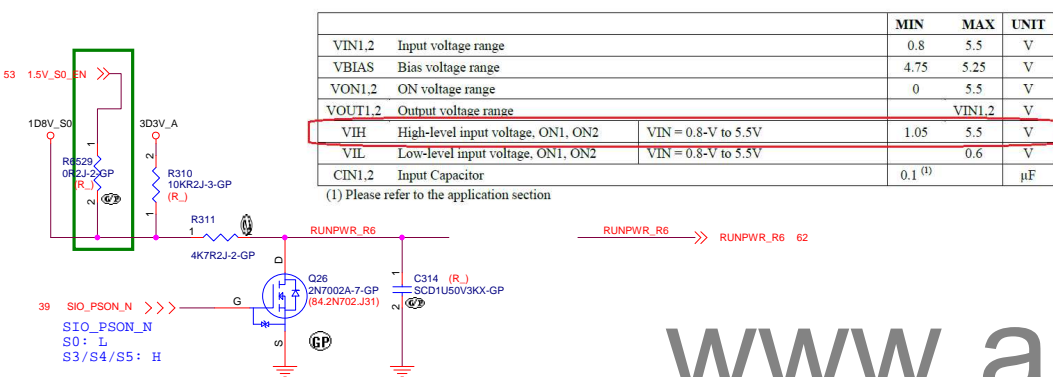






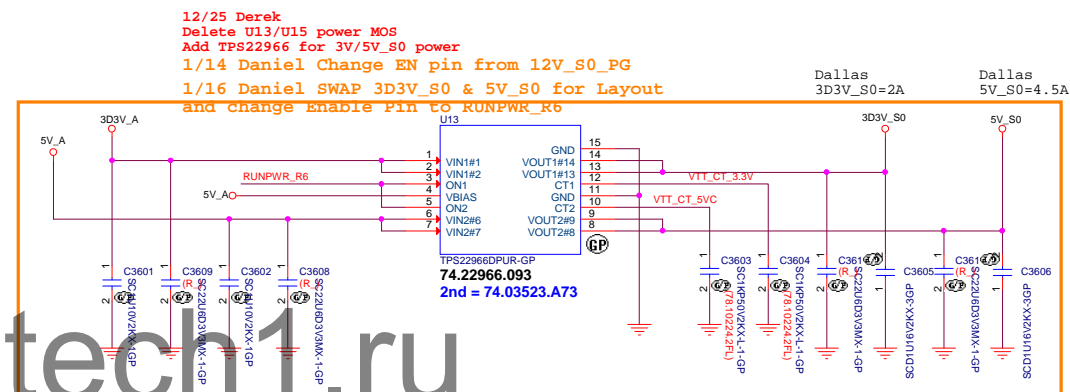
Without card	
Inserted card(lock)	
Inserted card(unlock)	

ANNIE Run Power



			MIN	MAX	UNIT
VIN1,2	Input voltage range		0.8	5.5	V
VBIAS	Bias voltage range		4.75	5.25	V
VON1,2	ON voltage range		0	5.5	V
VOUT1,2	Output voltage range		VIN1,2		V
VIH	High-level input voltage, ON1, ON2	VIN = 0.8-V to 5.5V	1.05	5.5	V
VIL	Low-level input voltage, ON1, ON2	VIN = 0.8-V to 5.5V		0.6	V
CIN1,2	Input Capacitor		0.1 ⁽¹⁾		μF

(1) Please refer to the application section



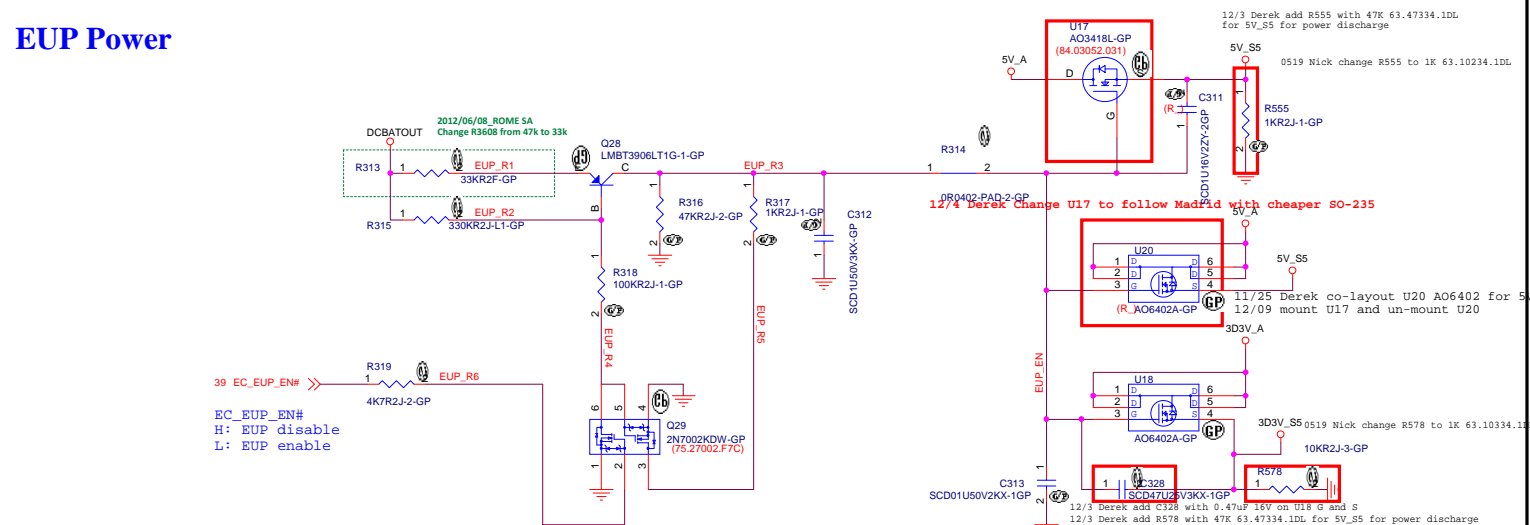
12/25 Derek
Delete U13/U15 power MOS
Add TPS22966 for 3V/5V_S0 power
1/14 Daniel Change EN pin from 12V_S0_PG
1/16 Daniel SWAP 3D3V_S0 & 5V_S0 for Layout
and change Enable Pin to RUNPWR_R6

Dallas	Dallas
3D3V S0=2A	5V S0=4.5A

closed to U13

2012/10/19 David
change from 84.04468.A37(11.6A,
to 84.06402.B3D(7A)

EUP Power



2012/10/21 David
Removed PS S3CNTRL

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Title	RUN POWER & SEQUENCE
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Size	Document Number	Rev
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AspireLink

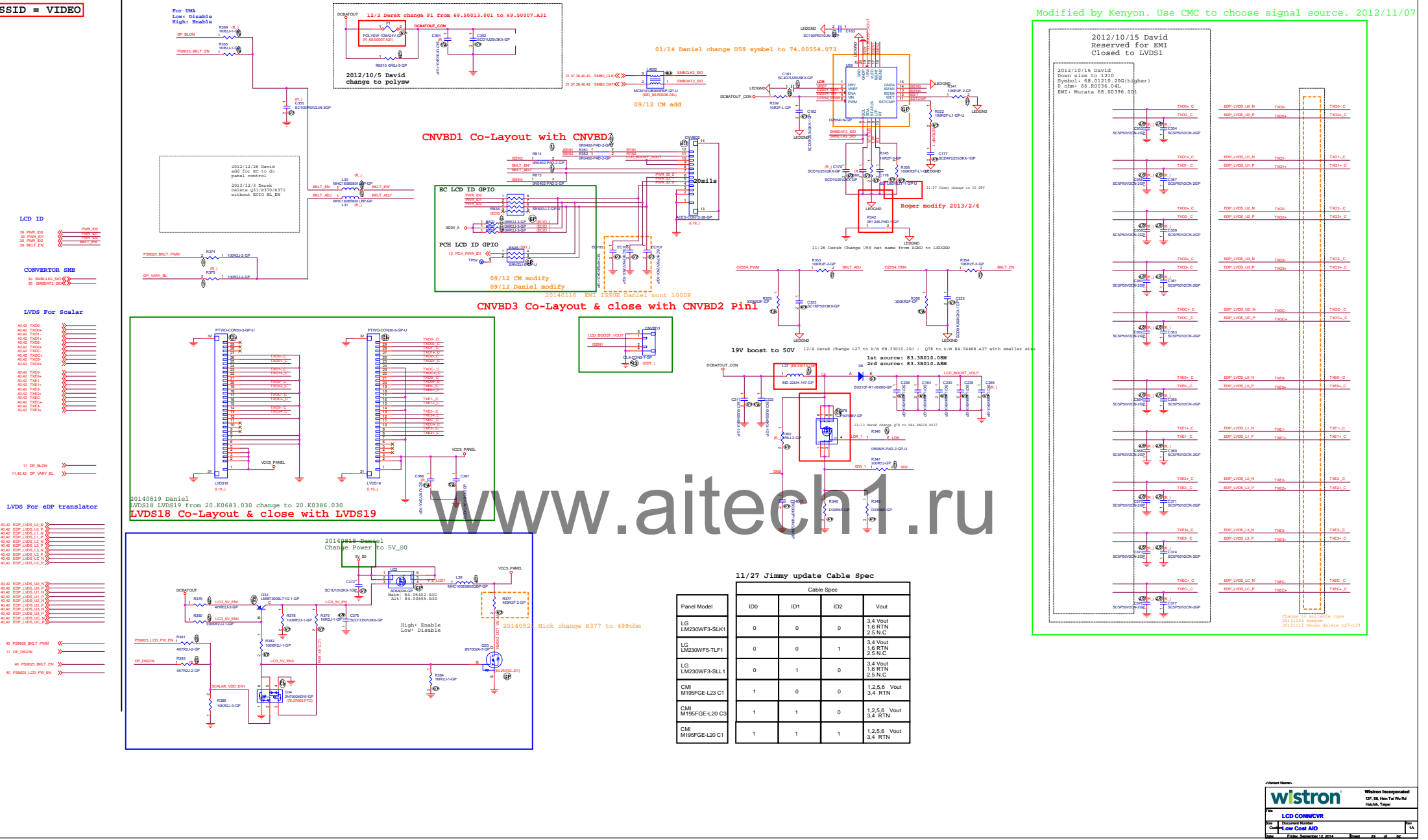
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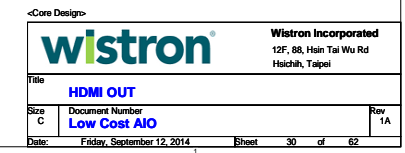
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Title AspireLink			
Size A	Document Number Low Cost AIO		Rev 1A
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SSID = VIDEO



Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
LG LM230WF3-SLK1	0	0	0	3.4 Vout 1.6 RTN 2.5 NC
LG LM230WF5-TLF1	0	0	1	3.4 Vout 1.6 RTN 2.5 NC
LG LM230WF3-SLL1	0	1	0	3.4 Vout 1.6 RTN 2.5 NC
CM1 M195FGE-L23 C1	1	0	0	1.2,5.6 Vout 3.4 RTN
CM1 M195FGE-L20 C3	1	1	0	1.2,5.6 Vout 3.4 RTN
CM1 M195FGE-L20 C1	1	1	1	1.2,5.6 Vout 3.4 RTN



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SATA HDD Connector

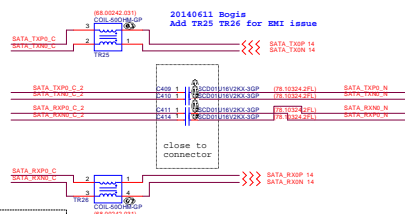
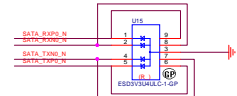
SIGNAL

Power segment pin 1

Pin 1

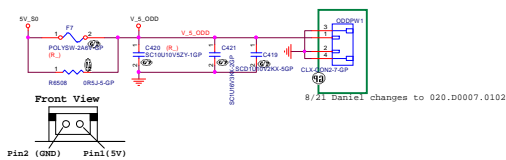
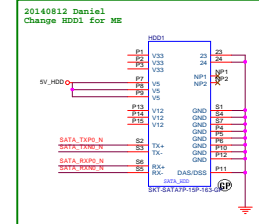
+3.3 VDC
+3.3 VDC
+3.3 VDC
GND
GND
+5 VDC
+5 VDC
+5 VDC
GND
GND
GND
+12V DC
+12V DC
+12V DC
15

SERIAL ATA POWER CONNECTOR

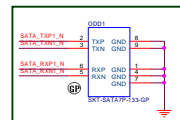
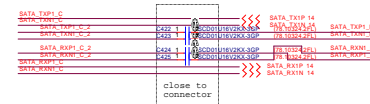


```
=====
          SATA_TXP0_C          SATA_TXP0_C_2
          SATA_TXN0_C          SATA_TXN0_C_2
          SATA_RXN0_C          SATA_RXN0_C_2
          SATA_RXP0_C          SATA_RXP0_C_2
=====
2012/10/5 David
Directly connected inside chip footprint for signal quality
(SA only!!!)
```

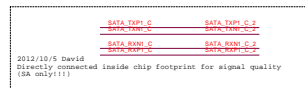
2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
If confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC



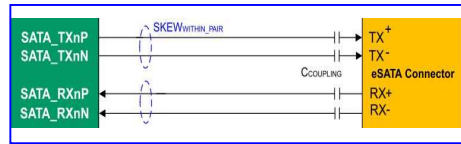
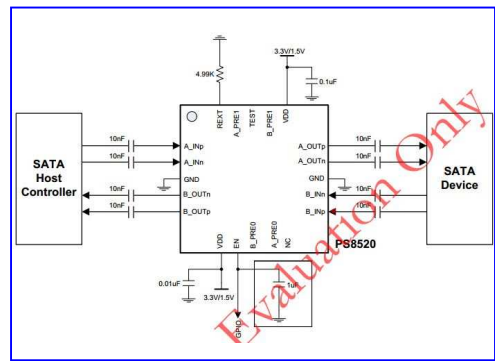
2013/05/21 David
Deleted SATA re-driver since
test PASS and to fix P/R issue



2012/10/24 David
EN pin and TEST pin can be floating for normal working.
Pin20 (REXT) should be connect to 4.99K ohm to GND



2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
If confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC

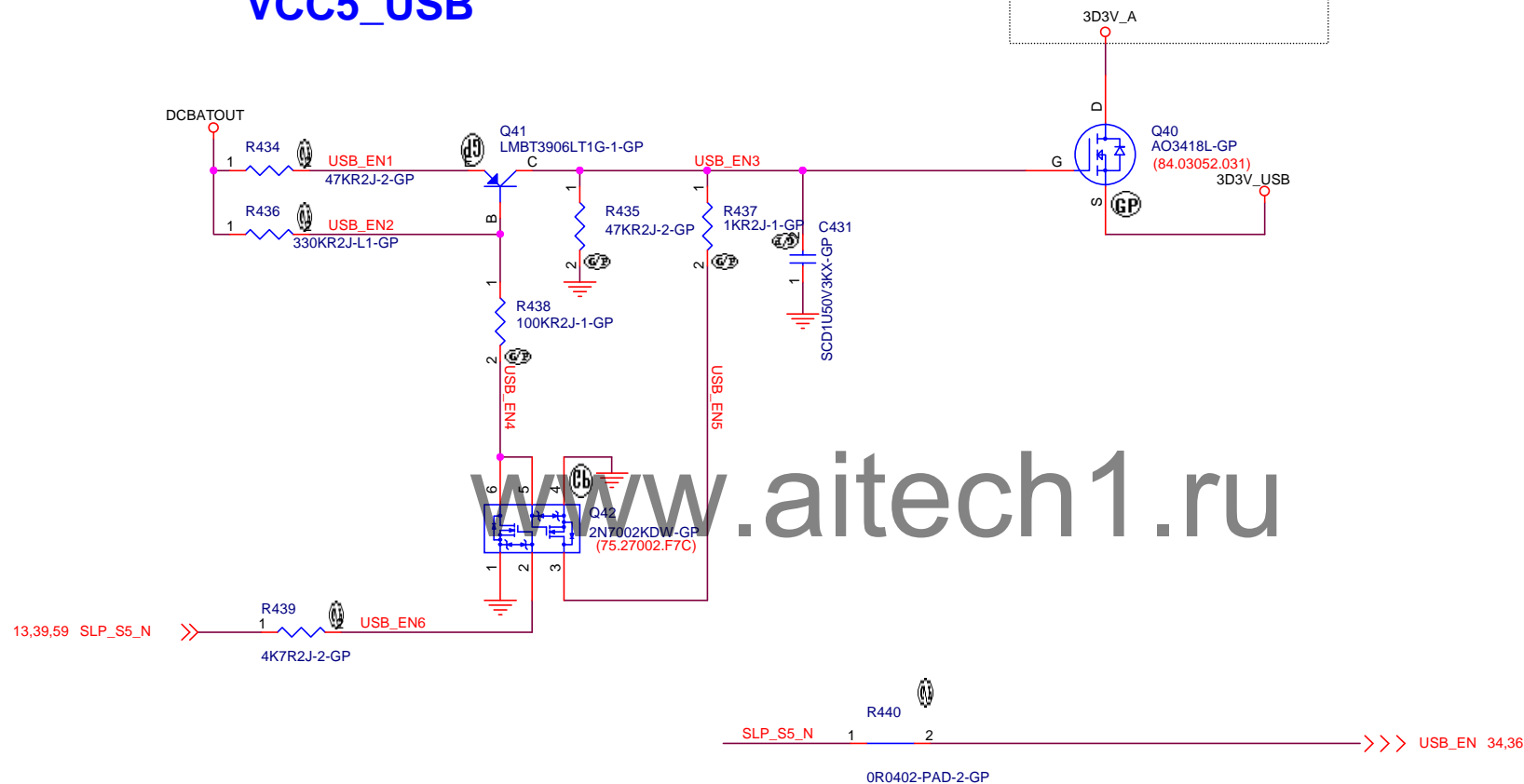


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SSID = USB

VCC5_USB

2012/11/10 David
Dallas change to 3D3V_A



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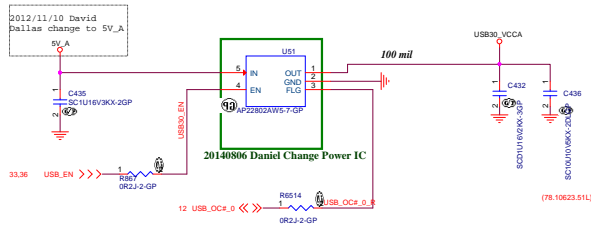
Title
USB 2.0 Power SW

Size Document Number
Custom **Low Cost AIO**

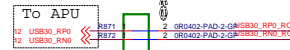
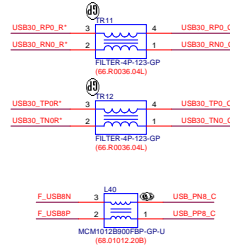
Rev
1A

Date: Friday, September 12, 2014 Sheet 33 of 62

20140508 Nick change F7 to 074.07549.0099

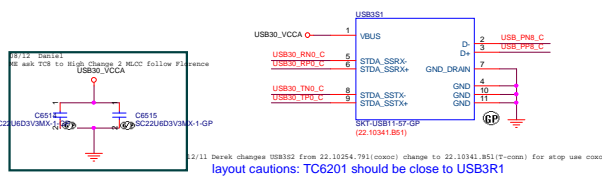
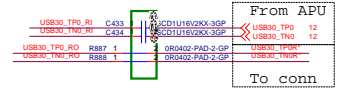


0ohm: 66.R0036.04L

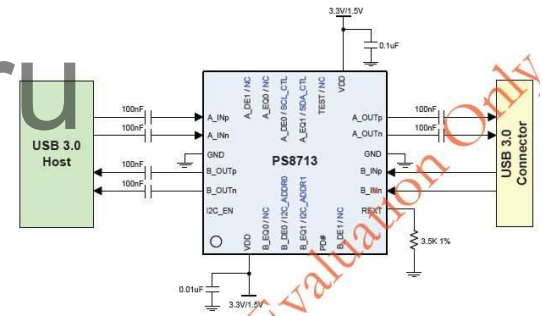
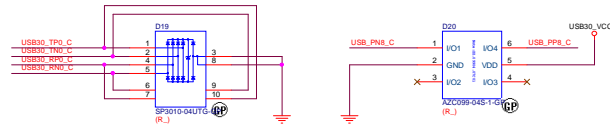
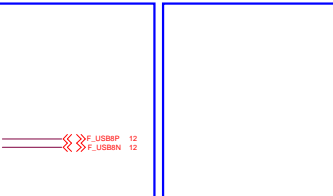


2012/07/12
If use NXIP
R126,R136= 0ohm
R81=NC
If use TI
R126,R136,R81= 0ohm

2012/10/5 David
Directly connected inside chip footprint for signal quality
(SA only!!!)

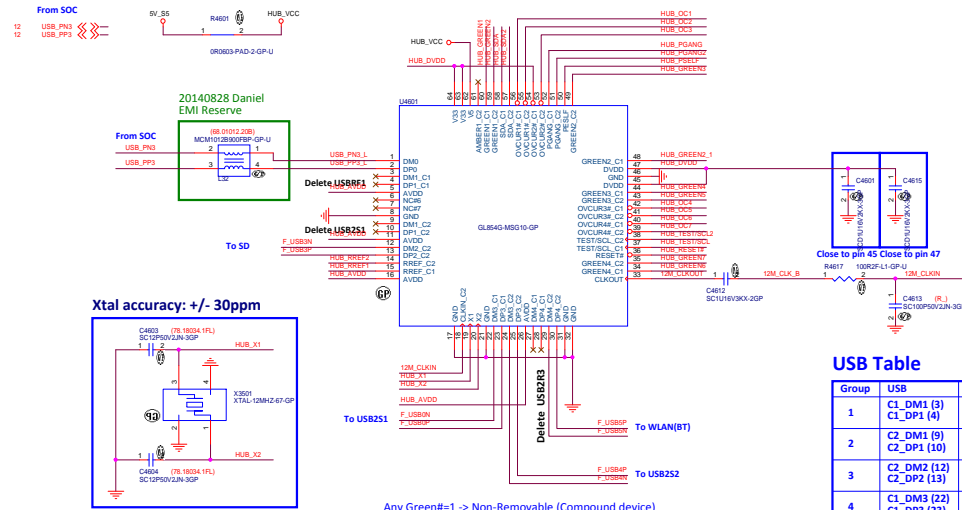


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX



GL850G
 Enable/Disable USB output port: D+/D- pull high 1K to disable USB port
 Set USB port to be internal (non-removable): set OC pin is floating
 Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

GL852G
 Enable/Disable USB output port: setting by EEPROM
 Set USB port to be internal (non-removable) or external (removable): setting by EEPROM

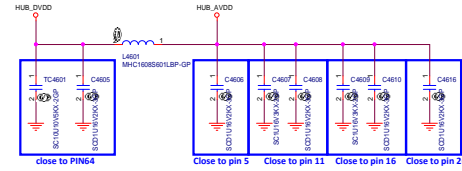


USB Table

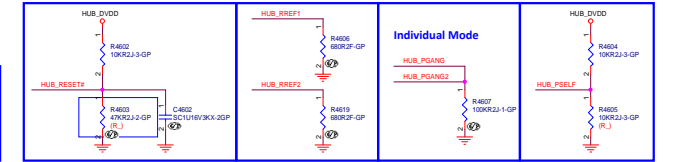
Group	USB	Device	
1	C1_DM1 (3) C1_DP1 (4)	USB251	Delete
2	C2_DM1 (9) C2_DP1 (10)	USB251	Delete
3	C2_DM2 (12) C2_DP2 (13)	SD	internal
4	C1_DM3 (22) C1_DP3 (23)	USB251	external
5	C2_DM3 (24) C2_DP3 (25)	USB252	external
6	C1_DM4 (27) C1_DP4 (28)	USB251	Delete
7	C2_DM4 (29) C2_DP4 (30)	MINI1	internal

36 F_USB4P USB2S2
 36 F_USB4P USB2S1
 36 F_USB4P MINI1
 37 F_USB4P SD

Internal Power
 (Hub Internal VR output from pin 63/64 V33 = HUB_DVDD)



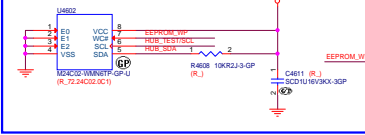
Fine tune resistor value for USB driving
 590ohm: 64.59005.6DL



HUB_PSELF = 1 if self-powered
 HUB_PSELF = 0 if bus-powered

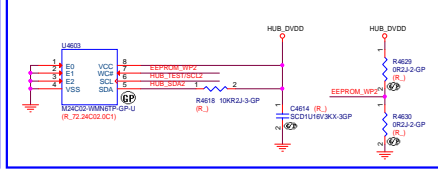
EEPROM

Option:
 24C02 for VID, PID,
 Strapping, Configuration.
 Option for 1-tier hub

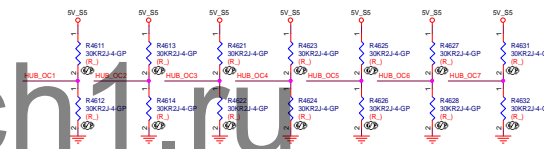


EEPROM

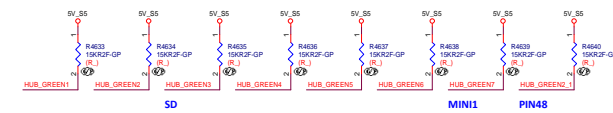
Option for 2-tier hub



Over Current

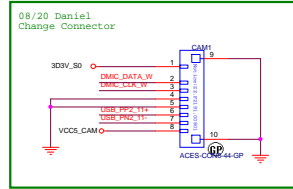
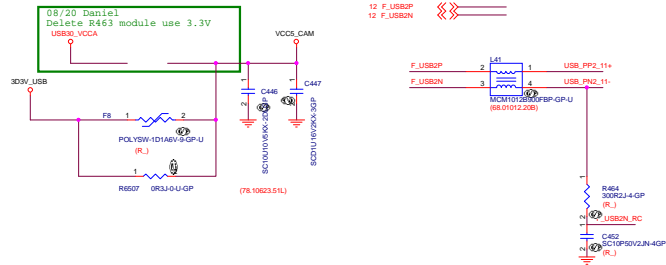


Green LED

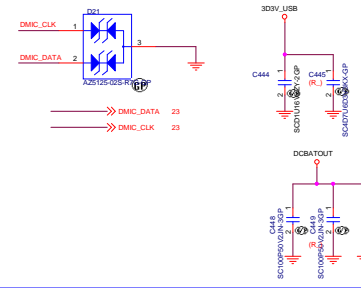


SSID =USB2.0

USB Port2 -> WEB CAM



DMIC Connector



USB Port 1 -> Delete TOUCH

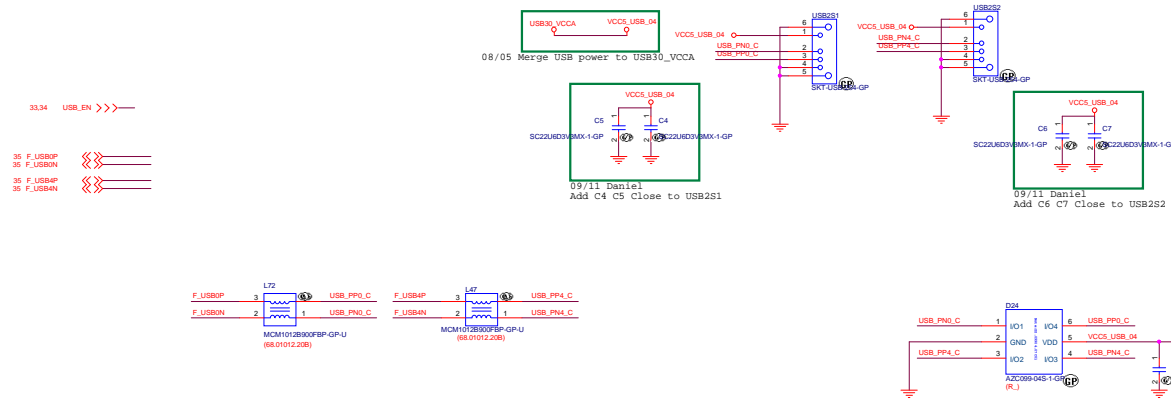
Max touch Connector Pin Define

PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

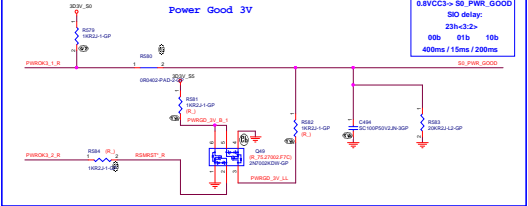
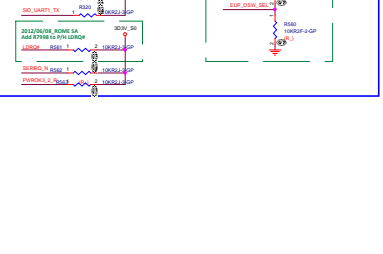
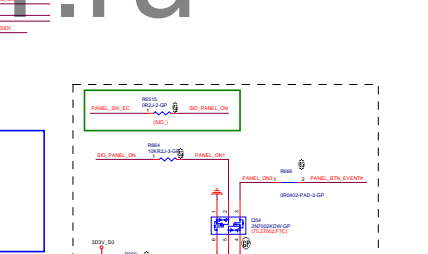
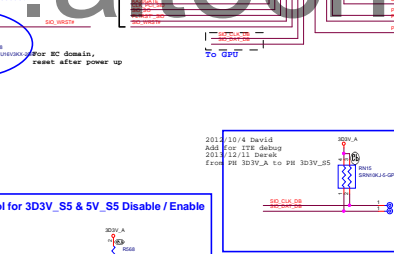
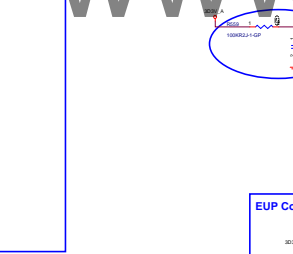
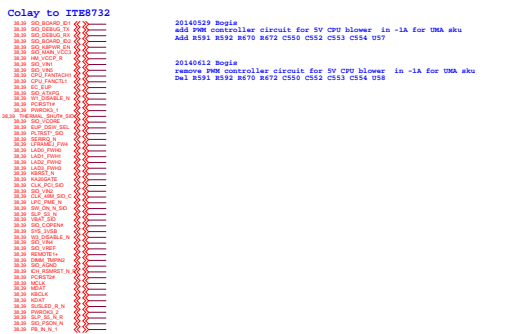
FX touch Connector Pin Define

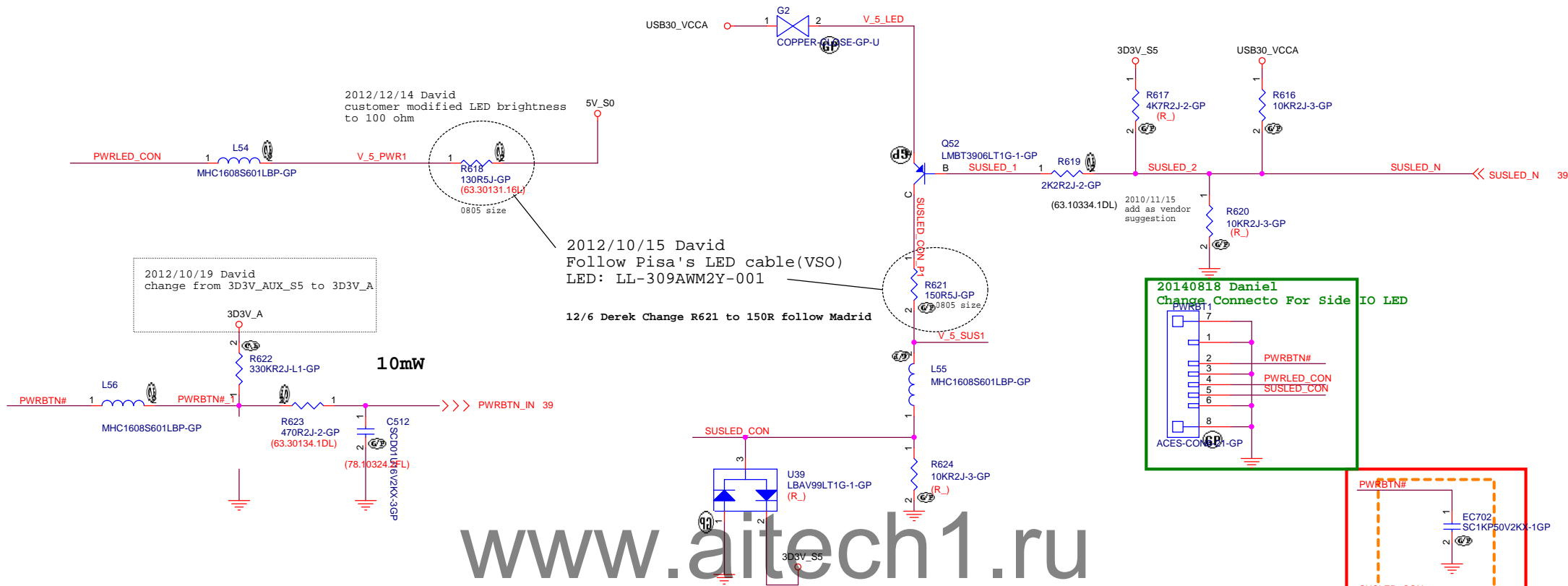
PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

USB Port -> Side I/O

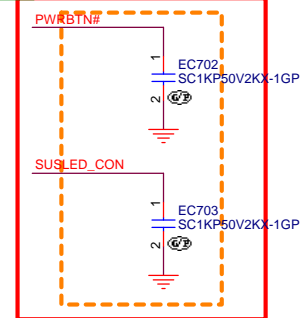
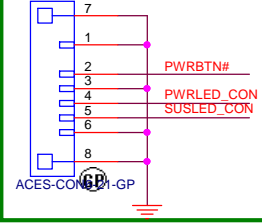






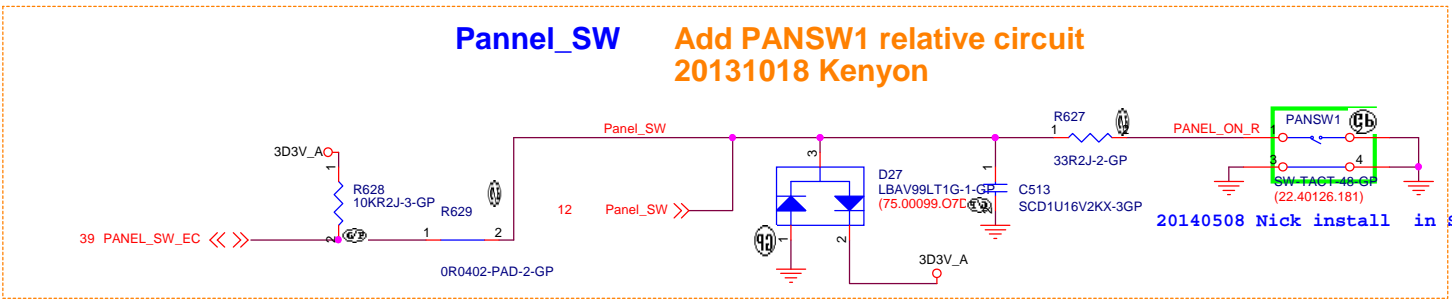


20140818 Daniel Change Connecto For Side IO LED




11/18 Akuan add dummy EC702/EC703
20140116 EMI ISSUE Daniel mont 1000P

Panel_SW Add PANSW1 relative circuit
20131018 Kenyon




20140508 Nick install in SB all SKU

<Variant Name>			
		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
PWRBTN / SIDE KEY / LED			
Size	Document Number		Rev
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Date:	Friday, September 12, 2014	Sheet	41 of 62

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<Variant Name>

		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title XDP			
Size B	Document Number Low Cost AIO		Rev 1A
Date:	Friday, September 12, 2014	Sheet	42 of 62

TBD

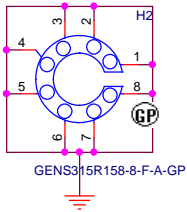
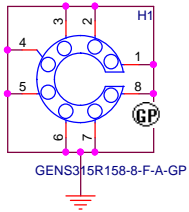
www.aitech1.ru

<Core Design>

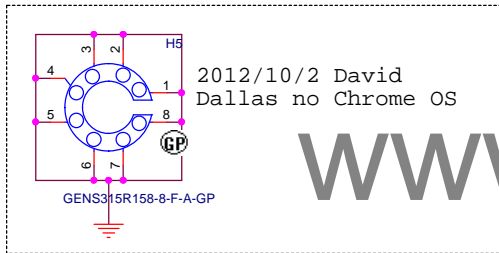
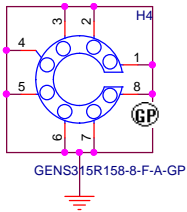
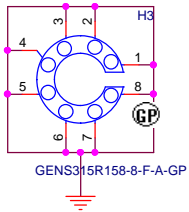


Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsinchu, Taipei

Title		SCALAR POWER	
Size	Document Number	Rev	
Custom	Low Cost AIO	1A	
Date: Friday, September 12, 2014		Sheet	43 of 62

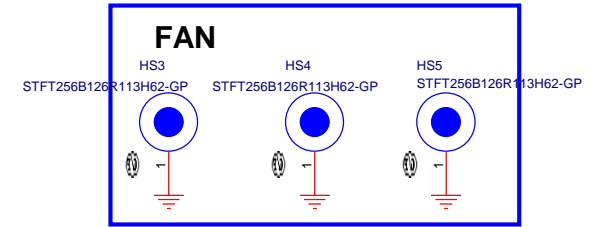
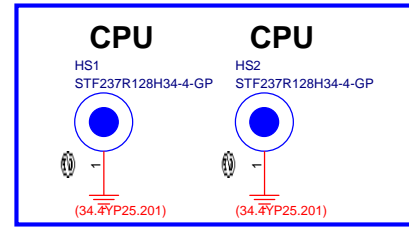


ZZ.SCREW.541



2012/10/2 David
Dallas no Chrome OS

www.aitech1.ru



<Core Design>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
STAND OFF / HOLE / EMI CAP

Size B Document Number
Low Cost AIO

Rev
1A

Date: Friday, September 12, 2014 Sheet 44 of 62

Material part

LGA115x CPU SOCKET Symbol

Vendor: LOTES
P/N: 22.78003.011

Vendor: FOXCONN
P/N: 22.78006.001

Vendor: LOTES
P/N: 22.78002.011
Thickness: max 2.2mm (含mylar及螺孔高)

Vendor: FOXCONN
P/N: 22.78006.011
Thickness: 2.0mm (含mylar)

Vendor: LOTES
P/N: 22.78005.171

Vendor: FOXCONN
P/N: 22.78005.161

2013/03/19 David
Removed CPU socket & back plate & cover

LABEL



LBL1
LABEL
(40.3BZ24.001)

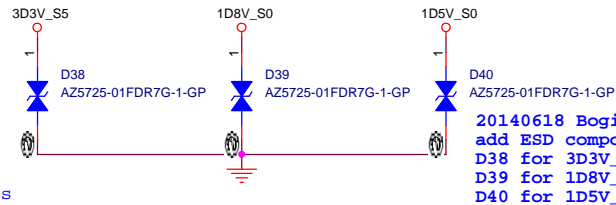


LBL2
LABEL
(R_)



LBL3
LABEL
(R_)

MB serial NO# and MAC address
40.3KP03.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm for aDallas
40.3BZ24.001 -> 30 x 15mm
09/24 Daniel
Change to 30x15 mm



Vendor: LOTES
P/N: 22.78005.171

Vendor: FOXCONN
P/N: 22.78005.161

HeatSink Symbol

2013/03/19 David
Removed HeatSink

Vendor
P/N:
60.3ET05.001
60.3ET05.011
60.3ET05.021

Battery Symbol



BTT2
BATTERY CR2032
(23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

PCB Symbol

2013/03/19 David
Removed Stand-off
since already exist

34.3KF01.001 for 5.2mm slot 62.10043.G11
34.3HJ03.001 for 9.0mm slot 62.10043.E41

<Core Design>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
HeatSink/Battery/etc

Size B Document Number
Low Cost A10

Rev
1A

Date: Wednesday, September 24, 2014 Sheet 45 of 62


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TBD


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<Core Design>

		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		GPU(2/5): IFB(10)	
Size	Document Number	Rev	
Custom	Low Cost AIO	1A	
Date:	Friday, September 12, 2014	Sheet	47 of 62

TBD

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<Core Design>			
		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
GPU(3/5): MEMORY FBA			
Size	Document Number		Rev
C	Low Cost AIO		1A
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TBD

GPI0	GP117
GPI0 0	FXM_PWMFB, CLAMP0B0US Service
GPI0 1	MEM_VDD_CTL
GPI0 2	UNUSED
GPI0 3	UNUSED
GPI0 4	UNUSED
GPI0 5	Reserved
GPI0 6	FB_CLAMP_TG1_REQ
GPI0 7	30Vmax(LUNSD)
GPI0 8	GPU Overtemp
GPI0 9	GPU Thermal Alert
GPI0 10	FB Hot Control
GPI0 11	NAVD0 PWM_M0D
GPI0 12	PWM_Low AC Drive
GPI0 13	UNUSEDB0 (Not to be used in H0B0)
GPI0 14	N/A on Package
GPI0 15	N/A on Package
GPI0 16	N/A on Package
GPI0 17	N/A on Package
GPI0 18	N/A on Package
GPI0 19	N/A on Package
GPI0 20	N/A on Package
GPI0 21	N/A on Package

Table 115. GB2-64 and GB4-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_M0H	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD V0D	MEM_VDD: Strap to boot FBVDD-Q
GPIO2	LCD_RL_PWM	O	Panel Backlight Pulse Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100K pull-down
GPIO4	LCD_RLH0	O	Panel Backlight Enable	100K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TG1_REQ	O	Active Low FB Clamp toggle request	
GPIO7	30Vmax	O	30-Vmax L/R signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	PWM_V0D	O	GPU Core VDD Pump control signal	
GPIO12	PWR_LVLH	I	AC power-good event, power supply overbrown input	100 K pull-up
GPIO13	PS	O	Thermal shutdown	10K pull-up to enable low phase
GPIO14	H0D_A	I	Hot Plug Detect for H0D used as DisplayPort or for H0D when used as Dual Link DVI	See Figure 76
GPIO15	H0D_C	I	Hot Plug Detect for H0C	See Figure 76
GPIO16	FBVDD_Q	I	J1 Frame Lock signal	See Figure 76
GPIO17	H0D_B	I	Hot Plug Detect for H0D	See Figure 76
GPIO18	H0D_E	I	Hot Plug Detect for H0E	See Figure 76
GPIO19	H0D_F or H0D_A	I	Hot Plug Detect for H0F or for H0D used as DisplayPort	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

• GPIO20 and GPIO21 are only available on H14M-GE/QL-HE/HS-B H14M-QV/QLV
• The unpopulated section of Table 107 indicates GPIOs that are not available for H14M-QV/QLV

GPIO0, GPIO6 are for G06 feature, no need to connect since this project won't support G06.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-Buses.
GPIO12: High-AC Mode/Low-Battery Mode enter slow down function/pull for power saving/Recommend Pull-High for AC mode.
GPIO13 PS: Change Phase from two to one, and then enter slow down function/pull for power saving.

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDDQ/FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/1.5 V	MT41J128M16JT-09GK	1000	1150	Production Candidate
				MT41J128M16JT-107G-K	900	1150	Production Candidate
	Samsung	0x5	1.5 V/1.5 V	K4V2G1646E-BC1A	1000	1204	Production Candidate
				K4V2G1646E-BC11	900	1204	Production Candidate
	Hynix	0x6	1.5V/1.5V	H5TQG63DFR-10C	1000	H/A	Production Candidate
				H5TQG63DFR-11C	900	H/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDDQ/FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
256Mx16 DDR3	Samsung	0x8	1.5 V/1.5 V	K4V4G1646B-HC11	900	H/A	Production Candidate
	Micron	0x0	1.5 V/1.5 V	MT41W256M16HA-107G-E	900	H/A	Production Candidate
	Hynix	0x3	1.5V/1.5V	H5TQ4G63MFR-11C	900	H/A	Production Candidate
				H5TQ4G63MFR-11C		H/A	Post-Production Candidate

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROH_SCLK	SUB_ALT_ADDR	10K Ω	Pull-down to GND
ROH_SI	SUB_VEN0R	10K Ω	Pull-up to 3V3 (if H0D5 ROM address)
ROH_SO	VGA_DEVICE	10K Ω	Pull-down to GND (if VGA device)
STRAP0	RAM_CFG[0]	10K Ω	See H0D below
STRAP1	RAM_CFG[1]	10K Ω	See H0D below
STRAP2	RAM_CFG[2]	10K Ω	See H0D below
STRAP3	RAM_CFG[3]	10K Ω	See H0D below
STRAP4	PCIE_MAX_SPEED	10K Ω	Pull-down to GND

Refer to the latest version of H14M-GE/QL Memory Recommended Vendor List for the specific setting for each memory type and configuration. Pull-up to 3V3 for binary "1" and pull-down to GND for binary "0".

XTAL

THERMAL PROTECTION

Mount	Un-mount	VRAM Type	P/N
R488 ~ R490 ~ R489 ~ R924	R483 ~ R486 ~ R929 ~ R934	Hynix 1G8s H5TC2063FPR-11C	KN.2GB00.038
R483 ~ R490 ~ R929 ~ R934	R488 ~ R486 ~ R489 ~ R924	MICRON 1G8s MT41J128M16JT-093G-K	KN.2GB04.022
R488 ~ R486 ~ R489 ~ R924	R483 ~ R486 ~ R929 ~ R934	SAMSUNG 1G K4W201646Q-BC1A	KN.2GB08.040

Mount 10K 64.10025.6DL

VRAM ID [0-3]	VRAM Type	P/N	0	1	2	3
Hynix 1G H5TC2063FPR-11C	KN.2GB00.038	V	V	V	V	V
72.52063.N0U		V	V	V	V	V

VRAM ID [0-3]	VRAM Type	P/N	0	1	2	3
Micron 1G MT41J128M16JT-093G-K	KN.2GB04.022	V	V	V	V	V
72.41128.10U		V	V	V	V	V

VRAM ID [0-3]	VRAM Type	P/N	0	1	2	3
SAMSUNG 1G K4W201646Q-BC1A	KN.2GB08.040	V	V	V	V	V
		V	V	V	V	V



KN.2GB08.041

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QVL1: Hynix (KN.2GB0G.038)+R221, R220, R231, R238 (64.10025.6DL)
QVL2: Micron (KN.2GB04.022)+R234, R238, R228, R219 (64.10025.6DL)

CHANNEL A:1GB DDR3

KN.2GB0G.038	2Gb	DDR3	128M*16	900MHz	SDRAM	FBGA96P	Hynix	-	H5TC2G63FFR-11C
KN.2GB04.022	2Gb	DDR3	128M*16	900MHz	SDRAM	FBGA96P	Micron	-	MT41J128M16JT-093G:K

VRAM Type	P/N
Hynix 1G H5TC2G63FFR-11C	KN.2GB0G.038
VRAM Type	P/N
Micron 1G MT41J128M16JT-093G:K	KN.2GB04.022

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FBCLK Termination place on VRAM side

128M*16 VRAM
KN.2GB0B.040 - Samsung K4W2G1646Q-BC1A
KN.2GB0G.038 - Hynix H5TC2G63FFR-11C

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Data Rate	Interface	Package
H5TC2G63FFR-11C	VDD/VDDQ=1.35V	900MHz	1.8Gbps/pin	SSTL-15	96ball FBGA
	VDD/VDDQ=1.5V	1.0Ghz	2.0Gbps/pin		
H5TC2G63FFR-11C	VDD/VDDQ=1.5V	1.1Ghz	2.2Gbps/pin		

Note) 1.35v speed part provides backward compatibility with the 1.5V DDR3.

RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

1. Ordering Information

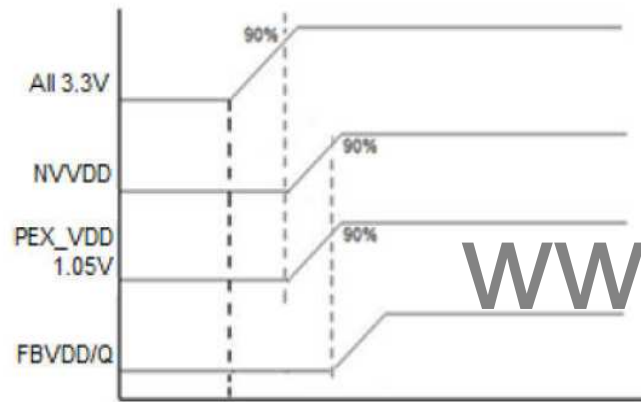
[Table 1] Samsung 128Mx16 Q-die ordering information table

Organization	gDDR3-1600(11-11-11)	gDDR3-1866(13-13-13) ²	gDDR3L-1866(13-13-13) ²	gDDR3-2133(14-14-14) ²	Package
VDD	1.5V	1.5V	1.35V	1.5V	
128Mx16	K4W2G1646Q-BC12	K4W2G1646Q-BC11	K4W2G1646Q-BC1A		96 FBGA

NOTE
1. Speed bin is in order of CL, RCD, WRP.
2. Backward Compatible to gDDR3-1800(13-13-13), gDDR3L-1800(13-13-13)
3. Backward Compatible to gDDR3-1800(13-13-13)

TBD

3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

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<Core Design>

wistron

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_POWER Sequence

Size B Document Number
Low Cost A10

Rev
1A

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TBD

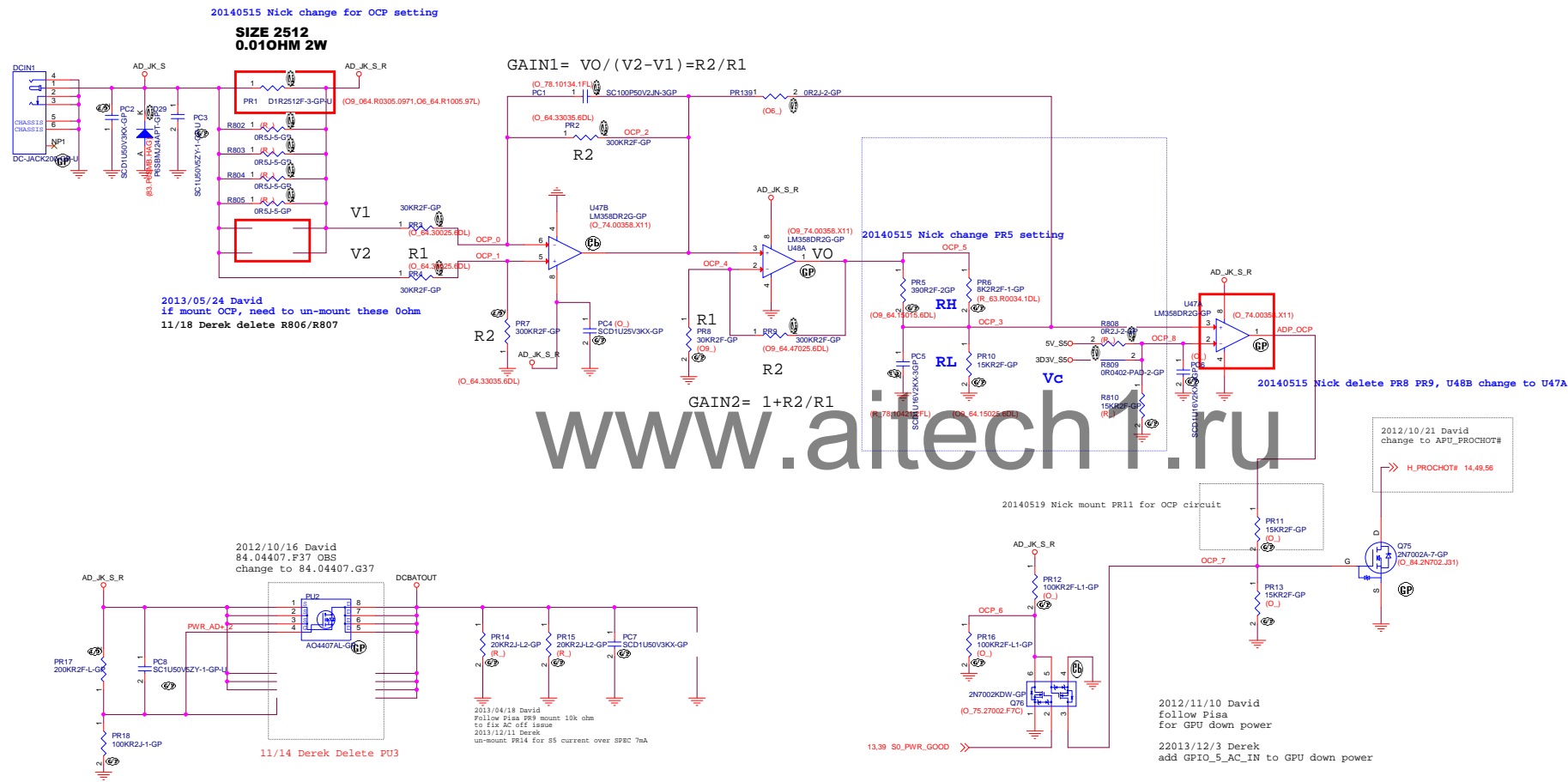
2014/4/29 Nick change from 5V_S0 to 5V_S5

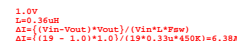
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ANNIE solution





3D3V_PWR / 5V_PWR

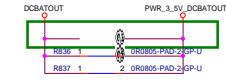


084.03319.0A37 SM3319
Vgs @ 4.5V,
Id = 7A,
Rds(on) = 23.0-30.0mohm,
Qg = 3.8-5.5nC

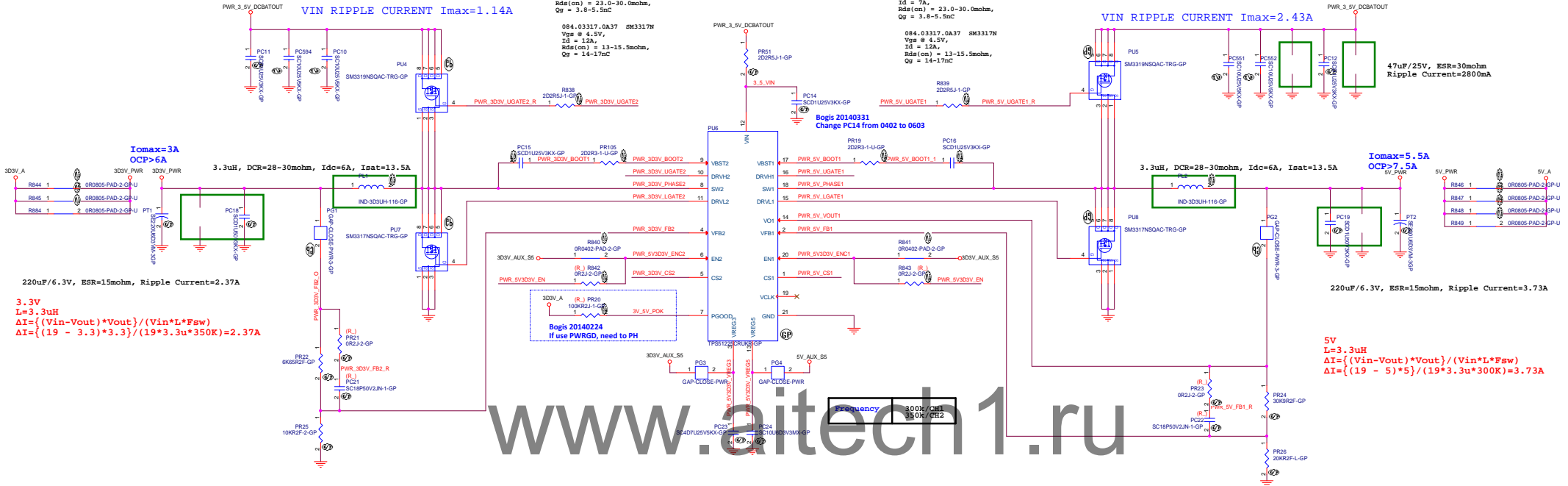
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Vgs @ 4.5V,
Id = 12A,
Rds(on) = 13-15.5mohm,
Qg = 14-17nC

084.03319.0A37 SM3319
Vgs @ 4.5V,
Id = 7A,
Rds(on) = 23.0-30.0mohm,
Qg = 3.8-5.5nC

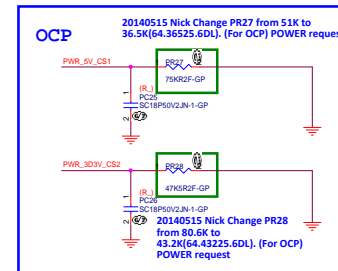
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Vgs @ 4.5V,
Id = 12A,
Rds(on) = 13-15.5mohm,
Qg = 14-17nC



47uF/25V, ESR=30mohm
Ripple Current=2800mA

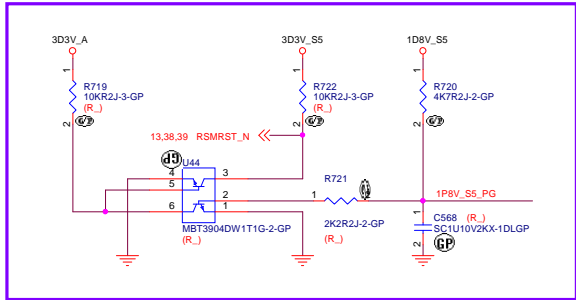


Frequency	300k/CH1 350k/CH2
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TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

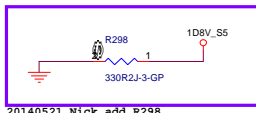
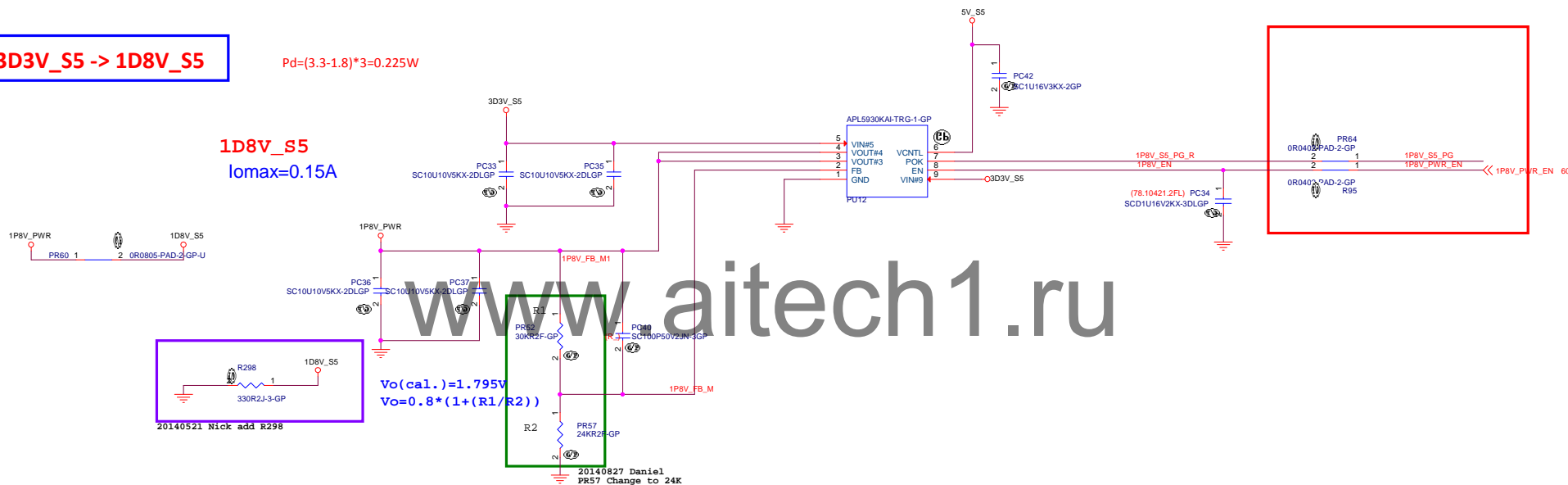
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only



3D3V_S5 -> 1D8V_S5

$$P_d = (3.3 - 1.8) \times 3 = 0.225W$$

1D8V_S5
I_{omax} = 0.15A



20140521 Nick add R298

$$V_o(\text{cal.}) = 1.795V$$

$$V_o = 0.8 \times (1 + (R1/R2))$$

20140827 Daniel
PR57 Change to 24K

<Core Design>

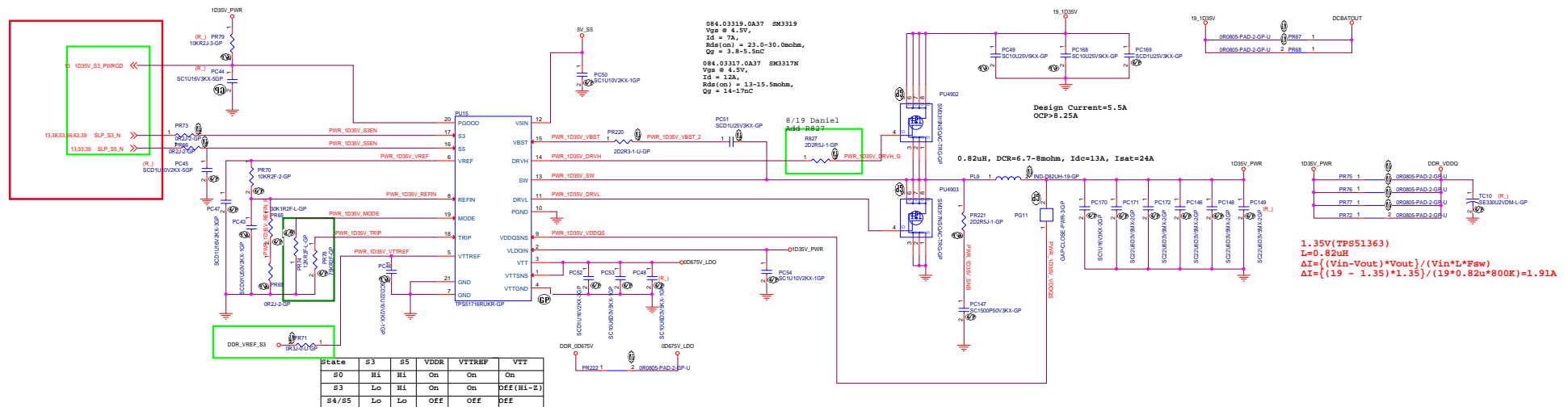
wistron		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsinchu, Taipei	
Title		PWR_1D8V_RT8237	
Size	Document Number	Rev	
Customer	Low Cost AIO	1A	
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DDR_1.35V

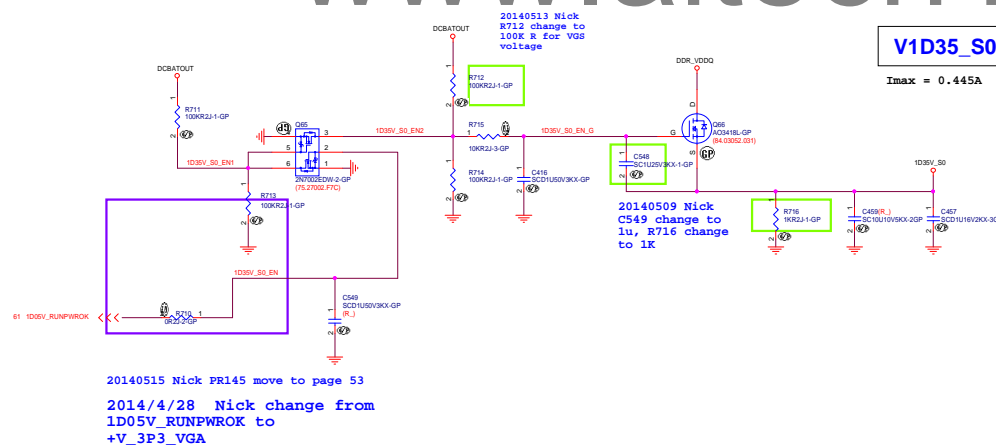
V_SM_VTT

EE need check

VIN RIPPLE CURRENT Imax=1.42A

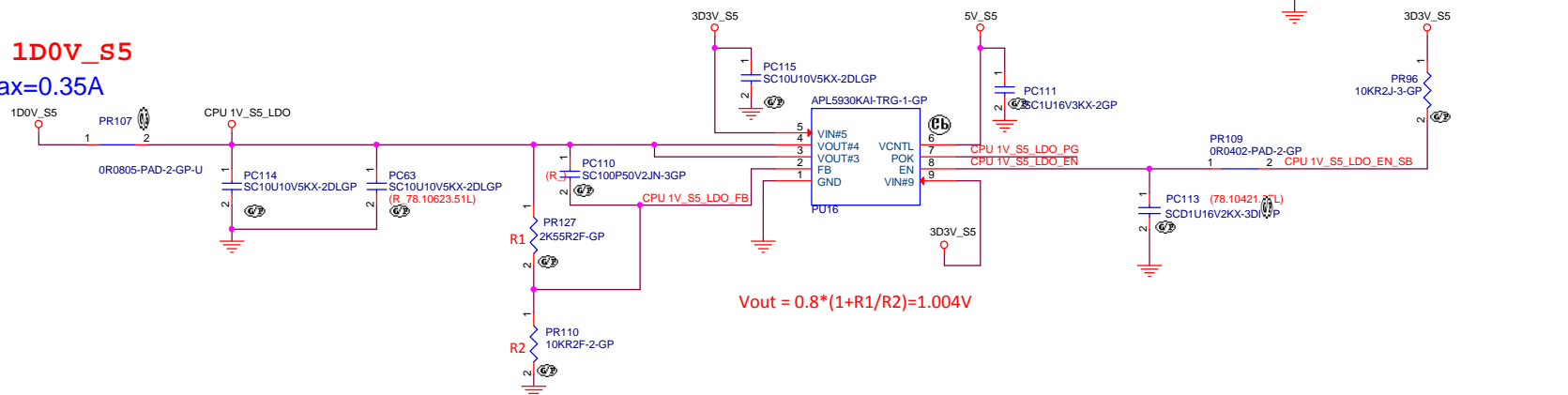


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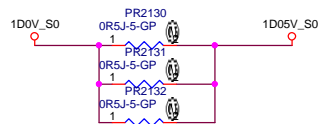


3D3V_S5 -> 1D0V_S5

CPU 1D0V_S5
I_{omax}=0.35A



Merger 1D05V_S0 -> 1D0V_S0



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<Core Design>

wistron

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Hsichih, Taipei

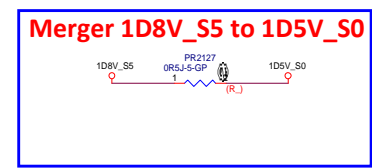
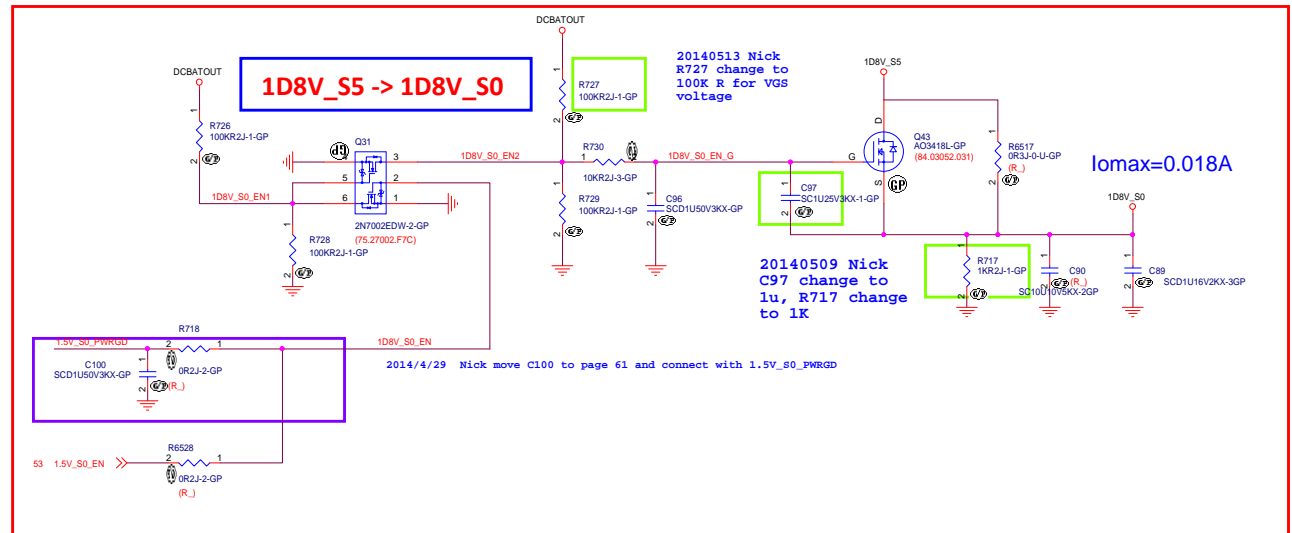
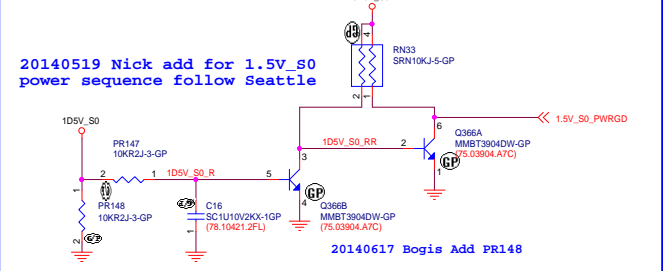
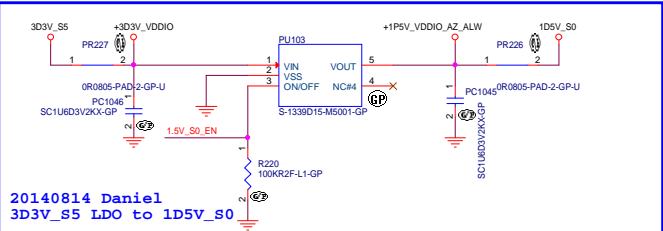
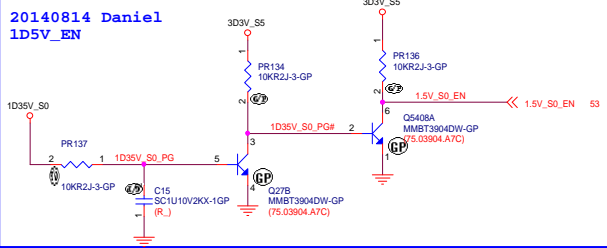
Title
PWR_CPU 1V_S0&CPU 1V_S5

Size
Custom

Date: Friday, September 12, 2014

Rev
1A

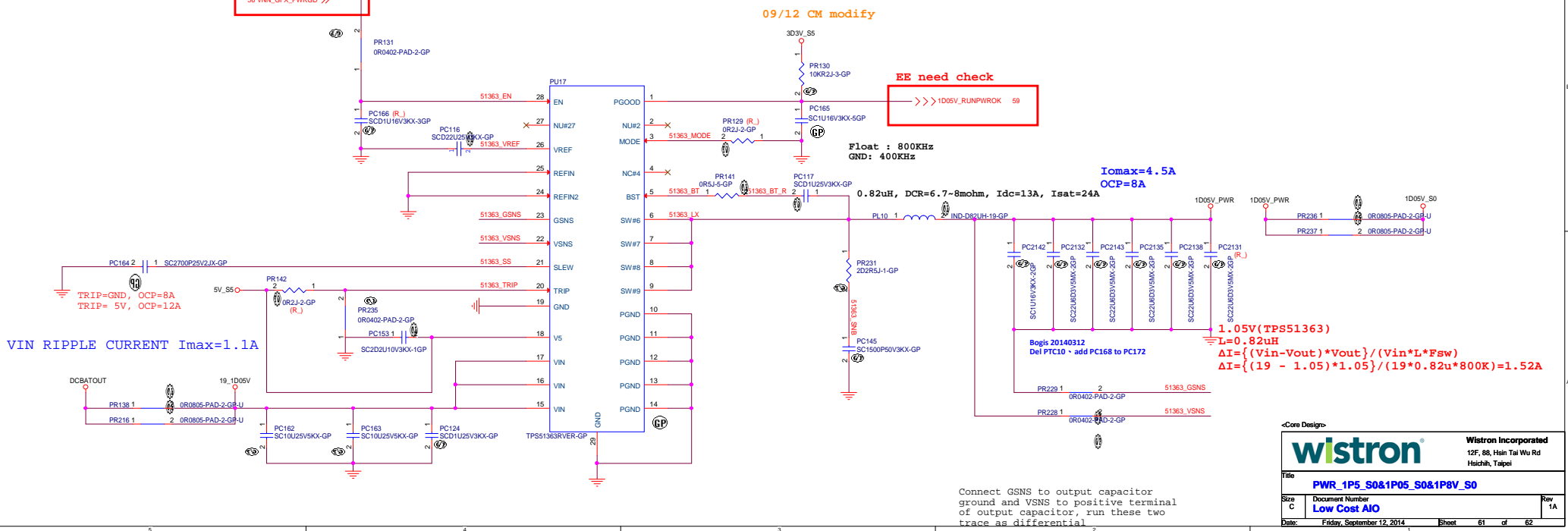
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1.05V
EE need check


56 VIN_GFX_PWRGD

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<Variant Name>



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Title

PWR_12V

Size

Document Number

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Sheet1

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